FIGURE 1.0

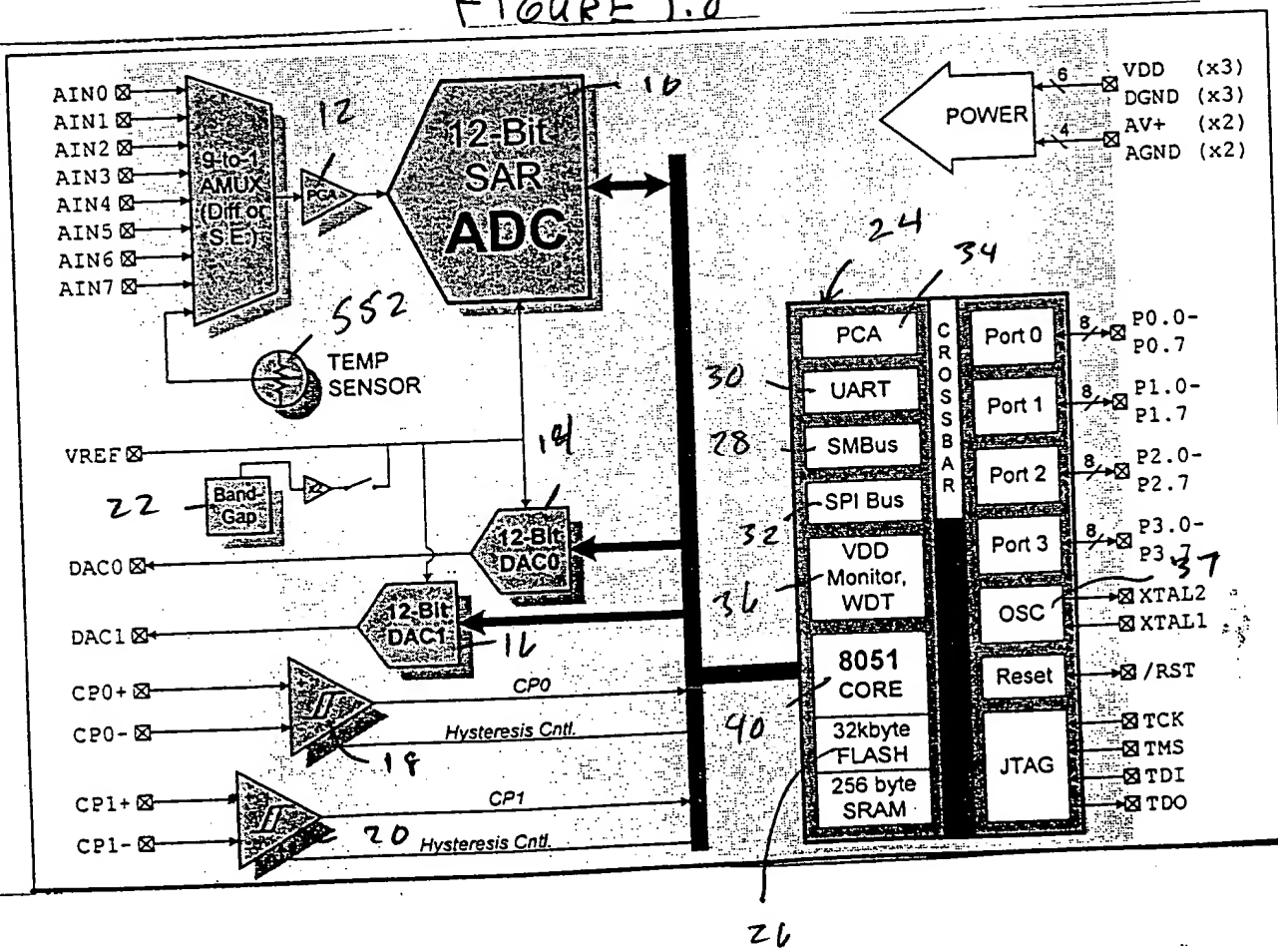
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
9-to-1 AMUX (Diff or S.E.)
PGA
12
12-Bit SAR ADC
16
552
TEMP SENSOR
VREF
Band Gap
22
18
12-Bit DAC0
12-Bit DAC1
DAC0
DAC1
16
CP0+
CP0-
CP0
Hysteresis Cntl.
18
CP1+
CP1-
CP1
20
Hysteresis Cntl.
POWER
6
4
VDD (x3)
DGND (x3)
AV+ (x2)
AGND (x2)
24
34
PCA
UART
SMBus
SPI Bus
VDD Monitor, WDT
8051 CORE
32kbyte FLASH
256 byte SRAM
30
28
32
36
40
CROSSBAR
Port 0
Port 1
Port 2
Port 3
OSC
Reset
JTAG
8
P0.0-P0.7
P1.0-P1.7
P2.0-P2.7
P3.0-P3.7
37
XTAL2
XTAL1
/RST
TCK
TMS
TDI
TDO
26

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Figure 1. C8051F000 Block Diagram

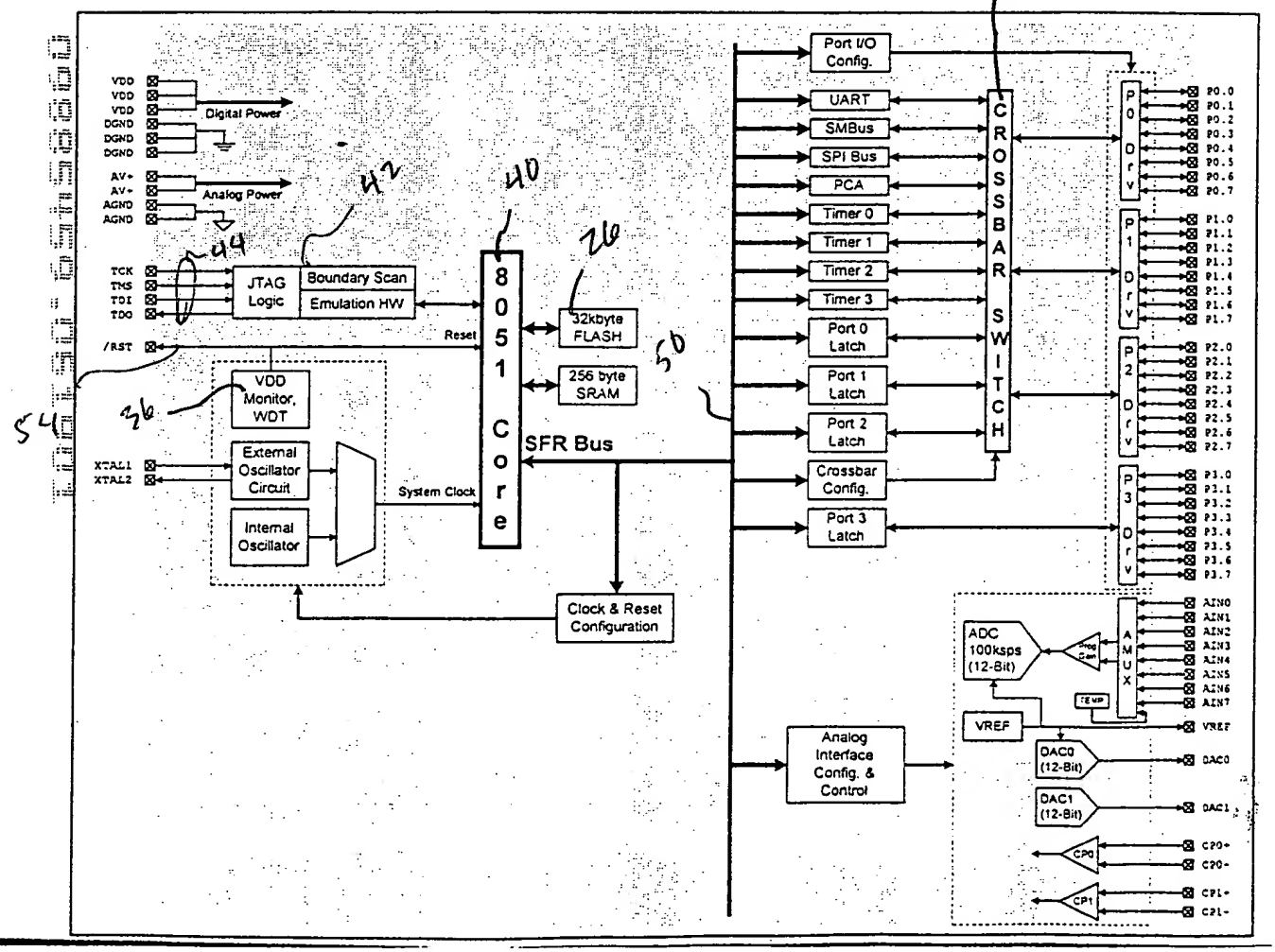

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Figure 1.3. On-Board Clock and Reset

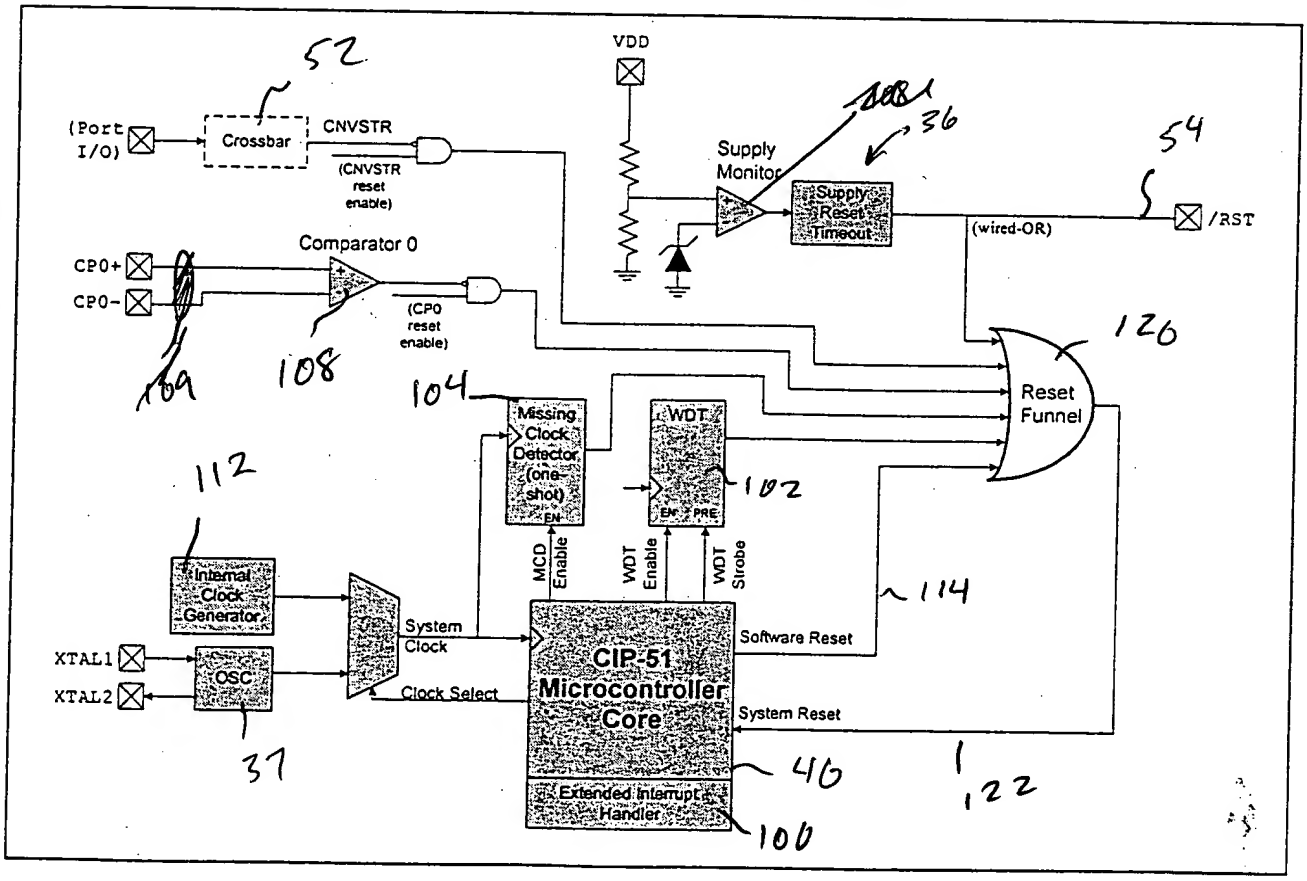

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Figure 1.4. On-Board Memory Map

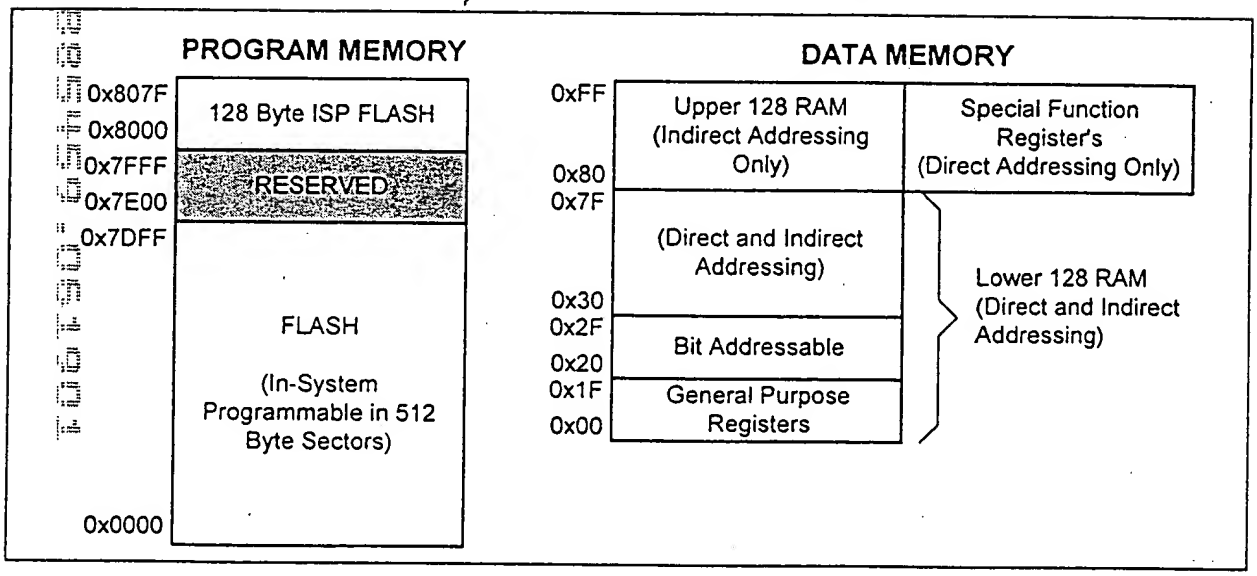


Figure 5. Emulation Diagram

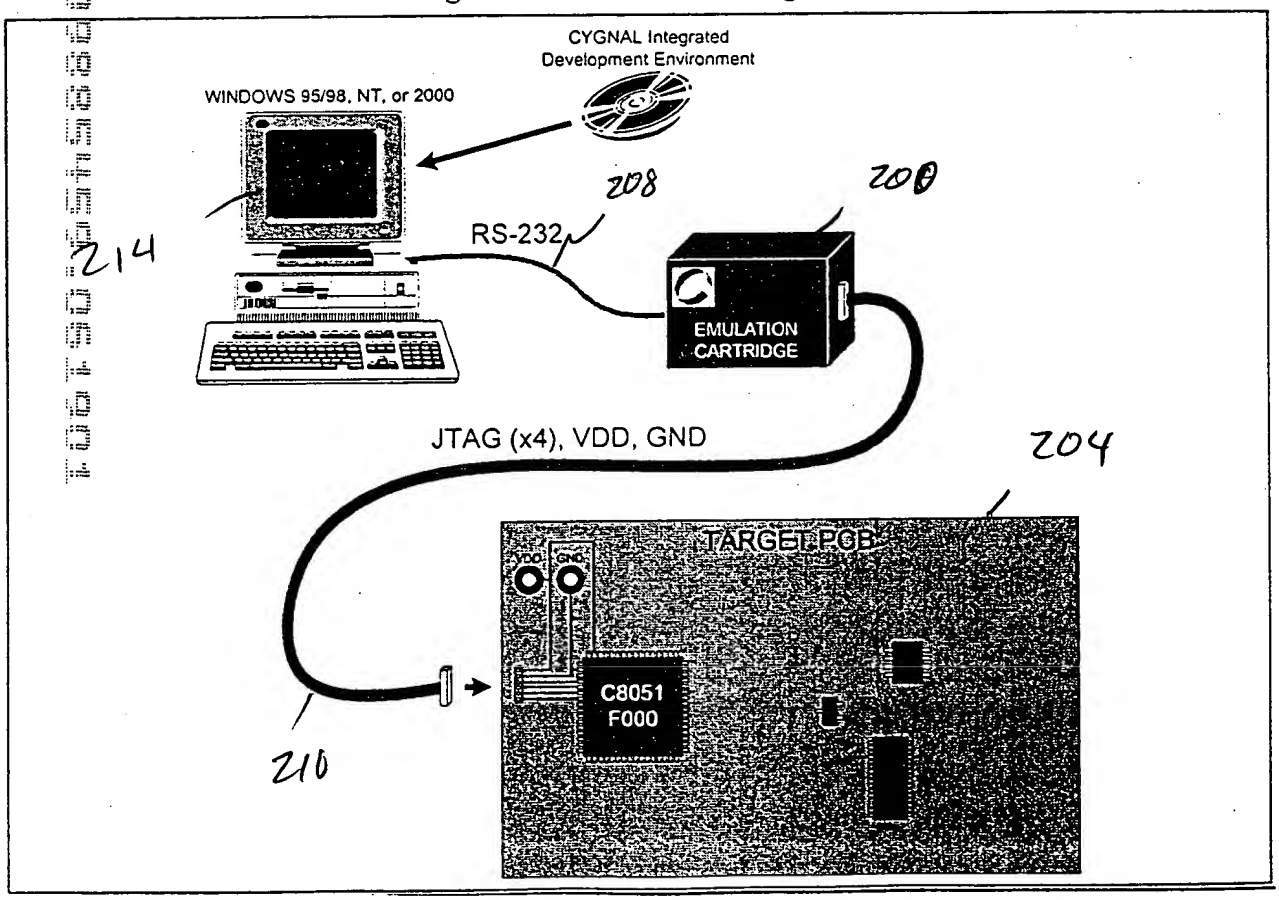
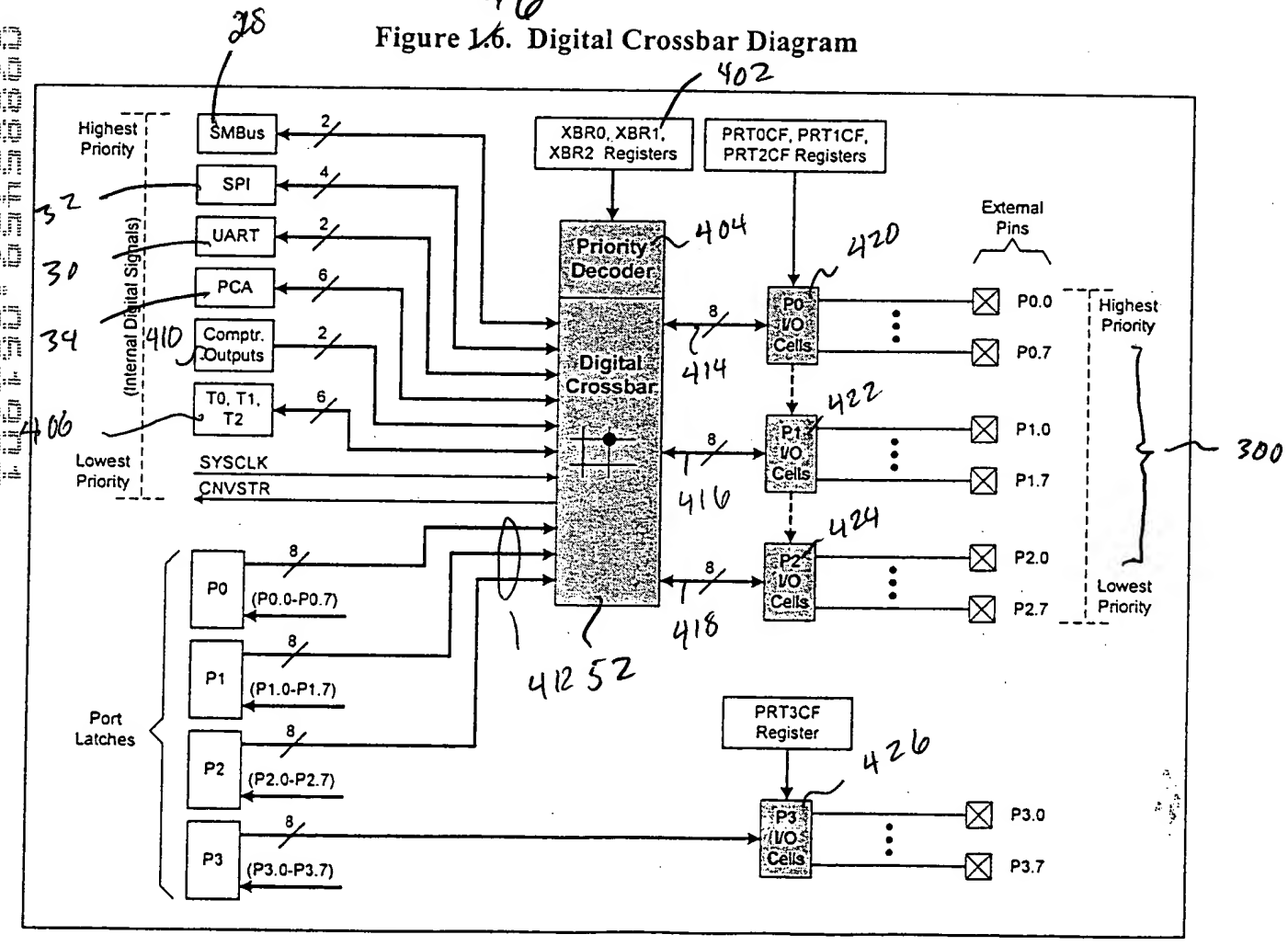


Figure 16. Digital Crossbar Diagram



& 7

Figure 17. PCA Block Diagram

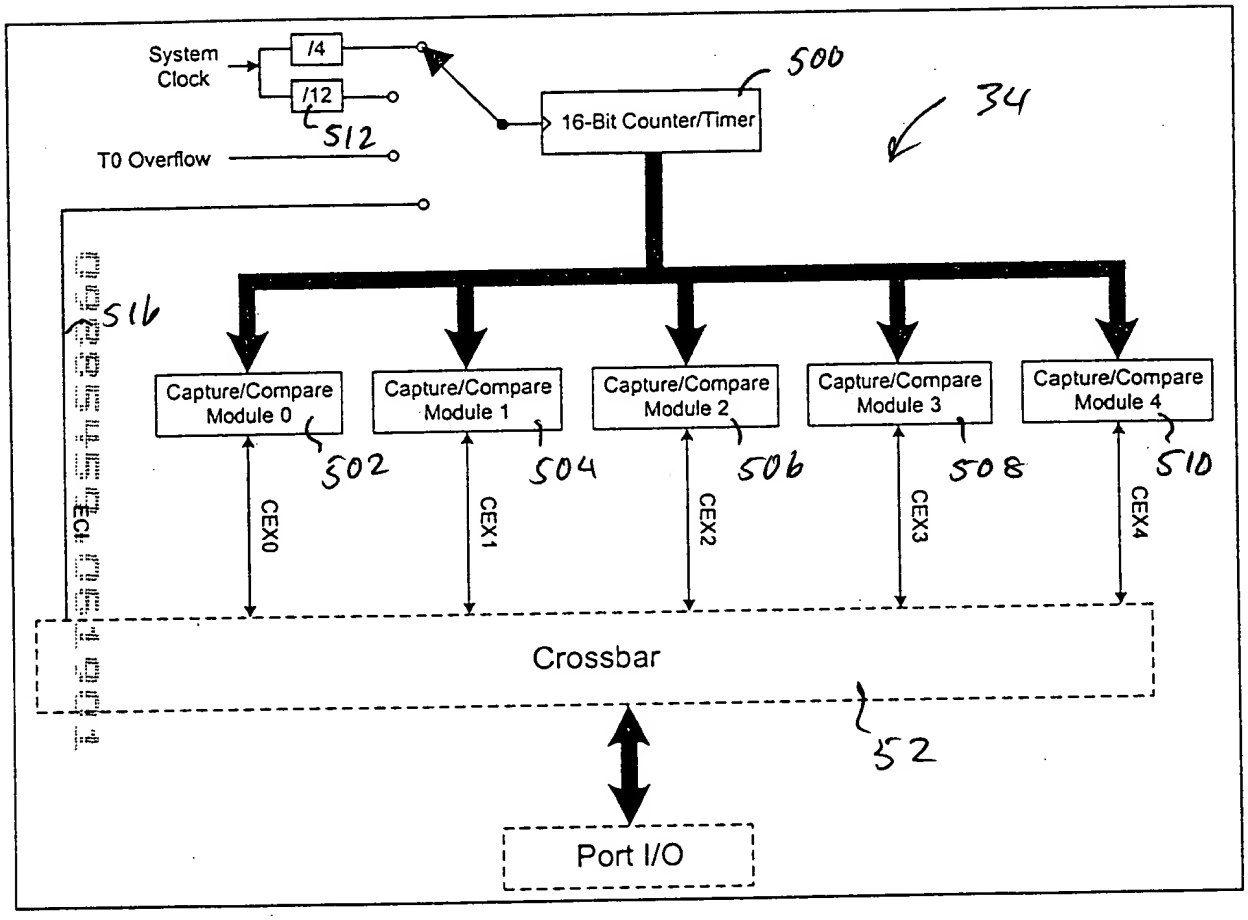


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Figure 1.8. ADC Diagram

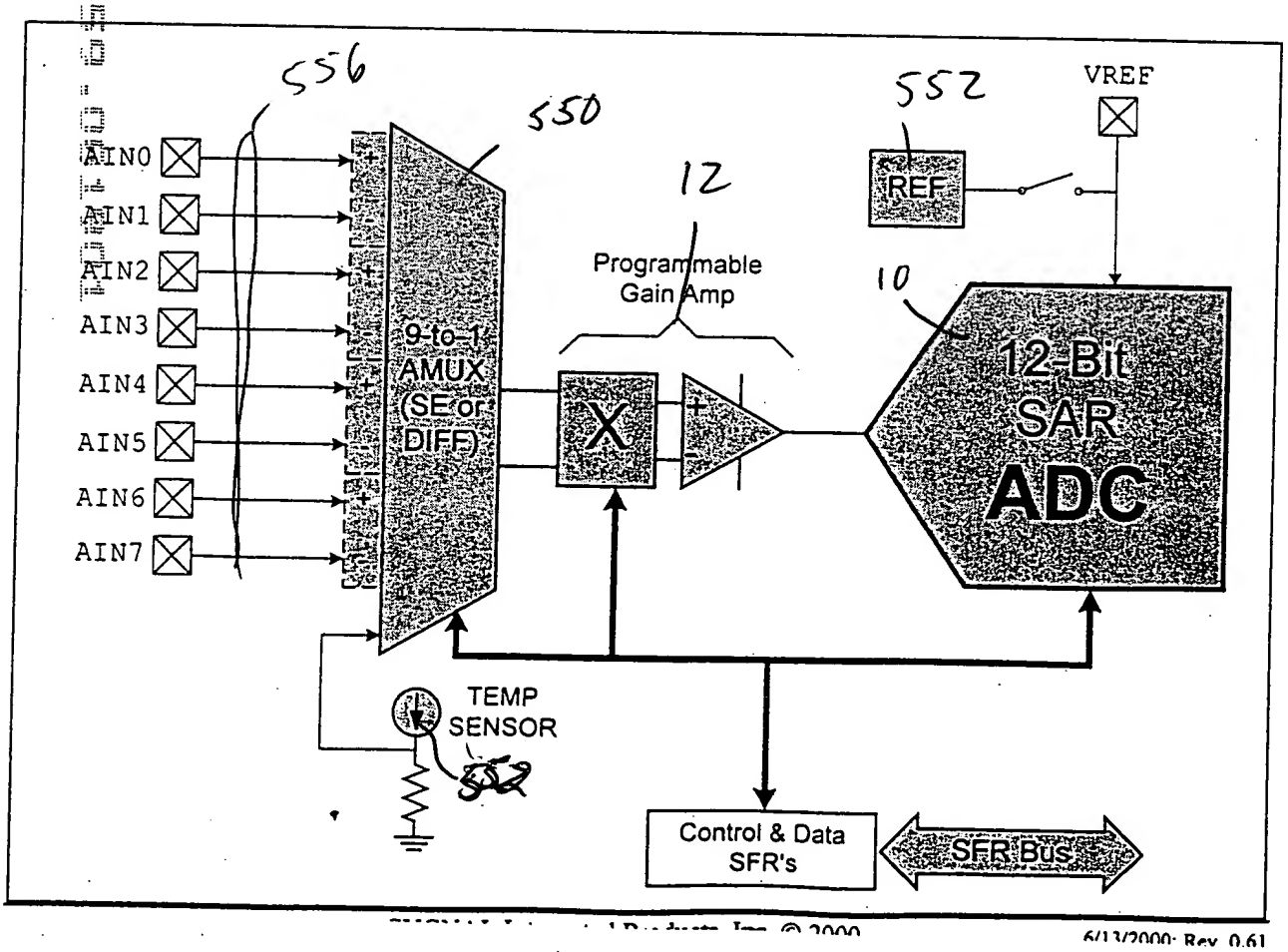

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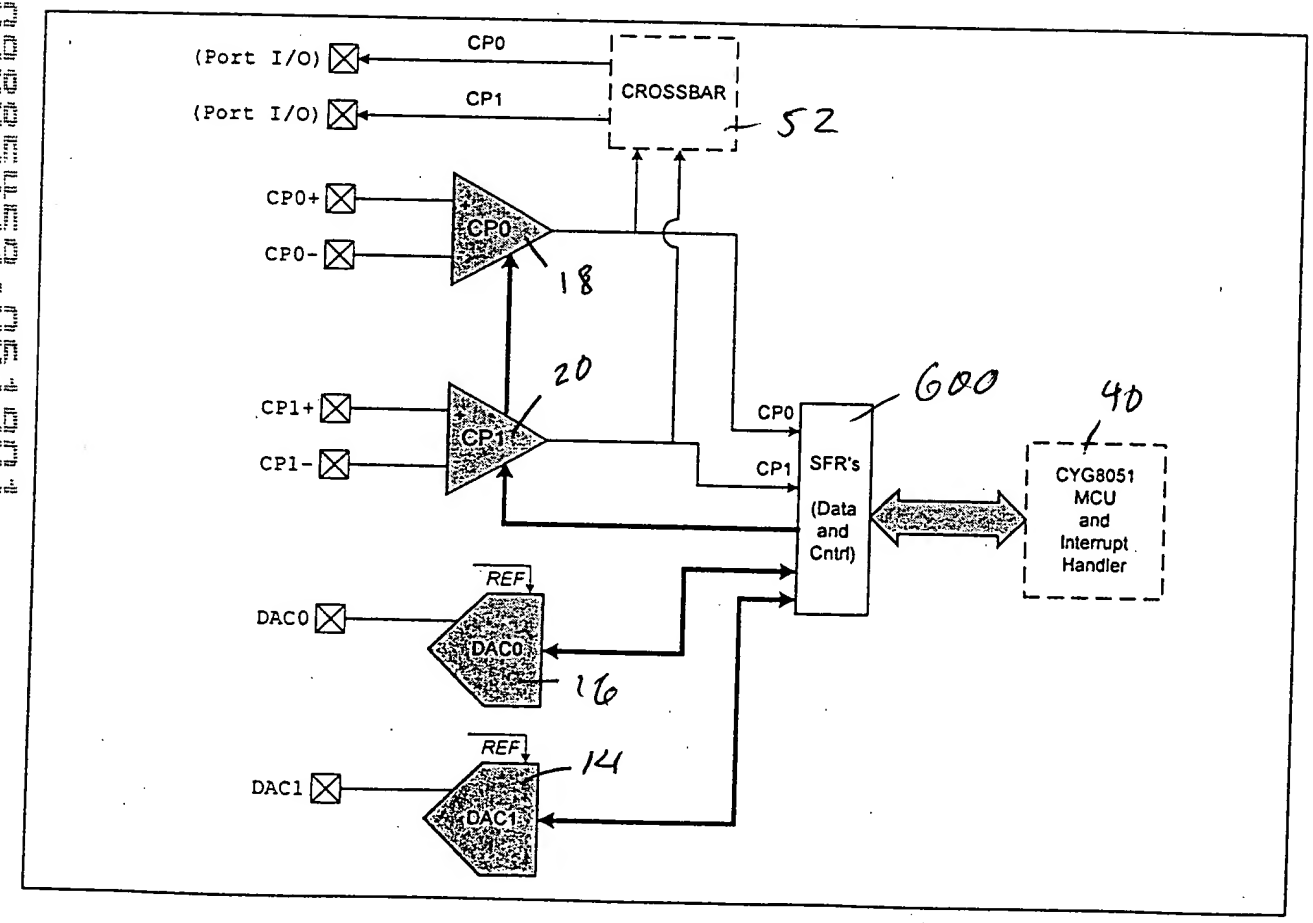
Figure 1.9. Comparator and DAC Diagram



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0.

Figure 5.1. ADC Functional Block Diagram

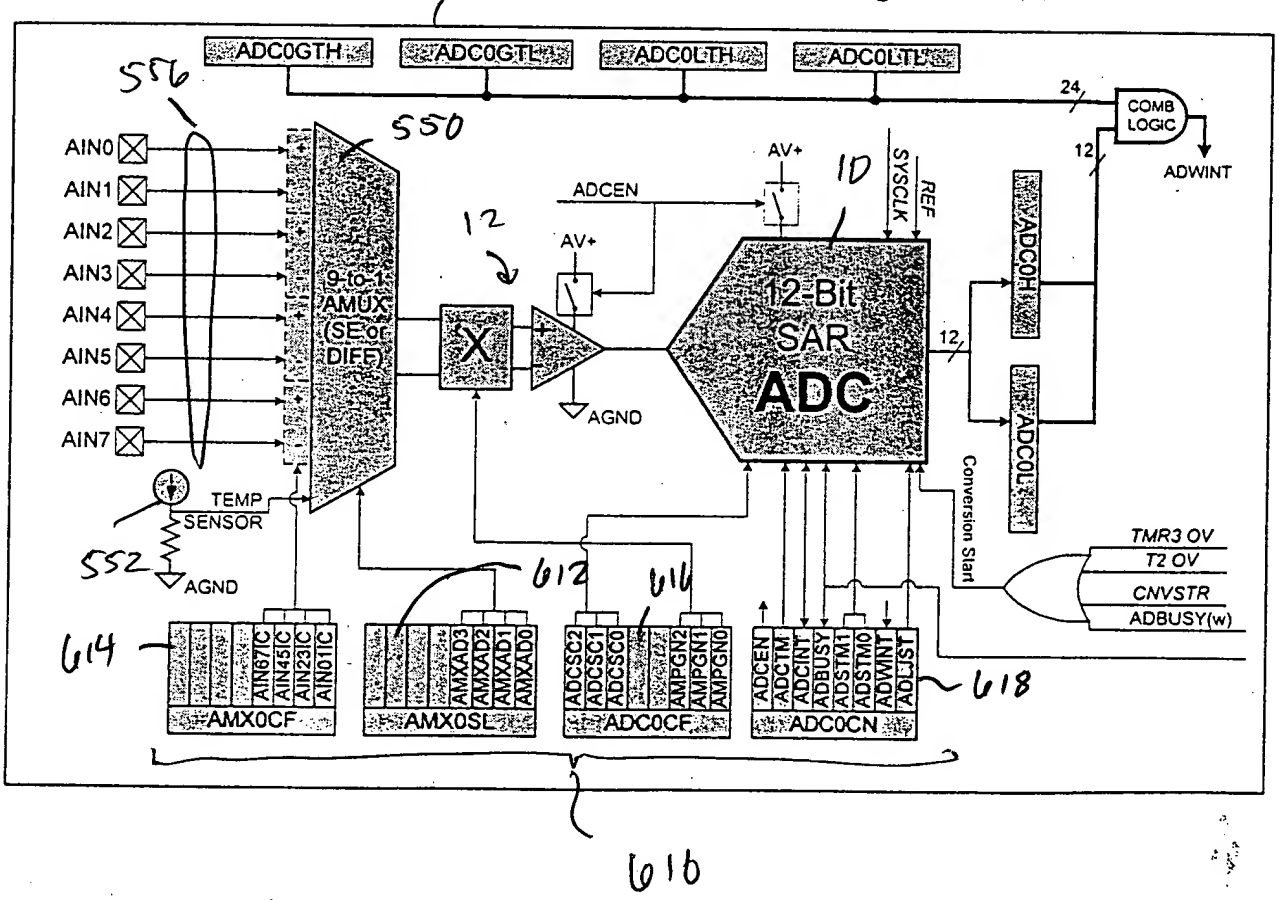

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Figure 5.2. ADC Track and Conversion Example Timing

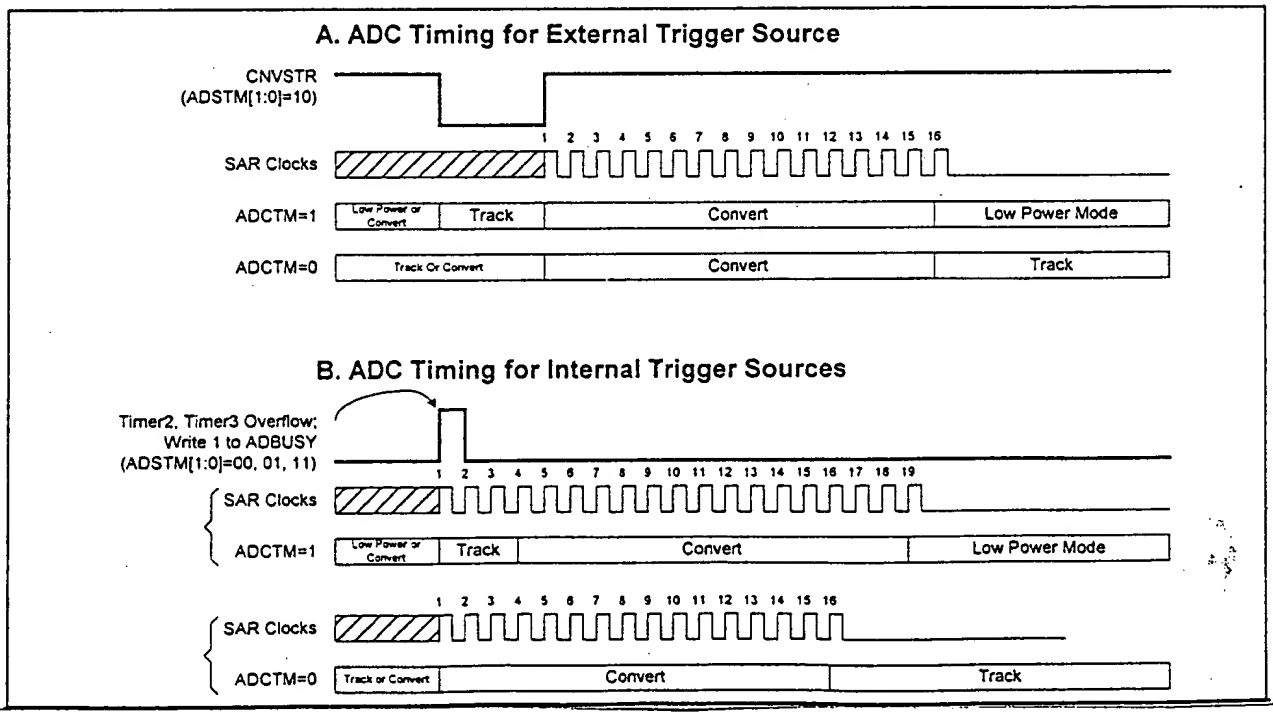

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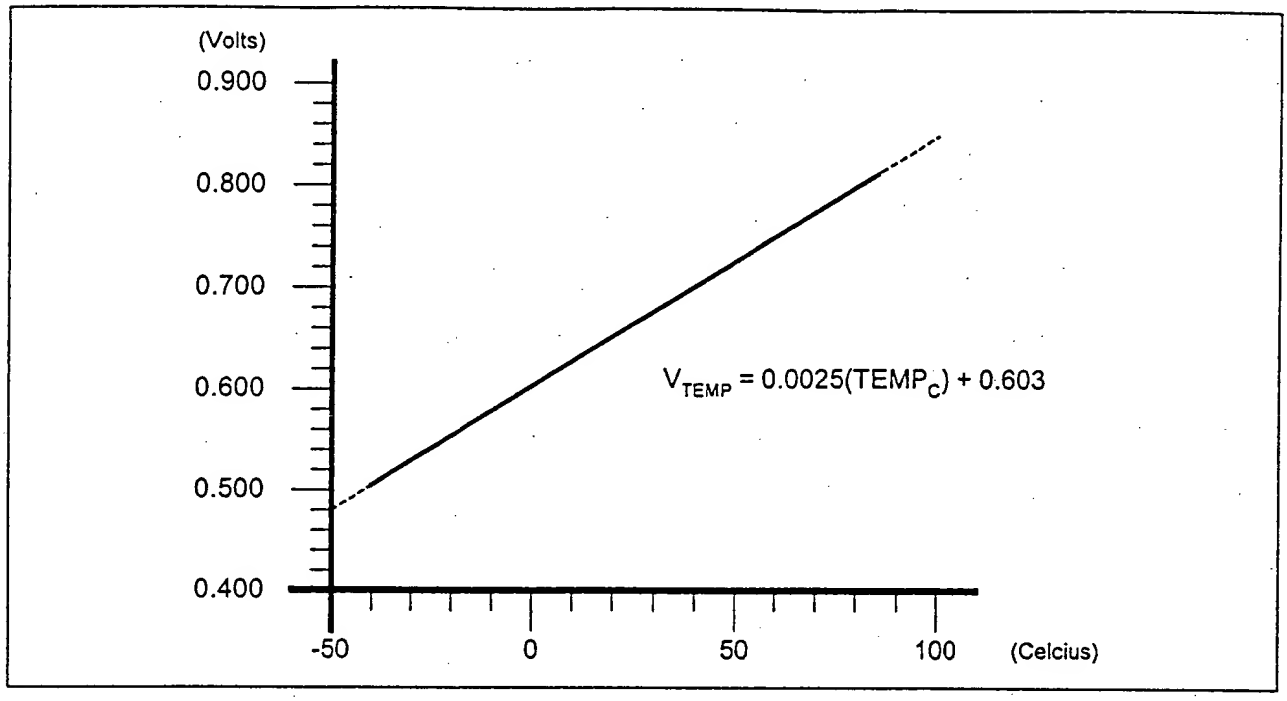
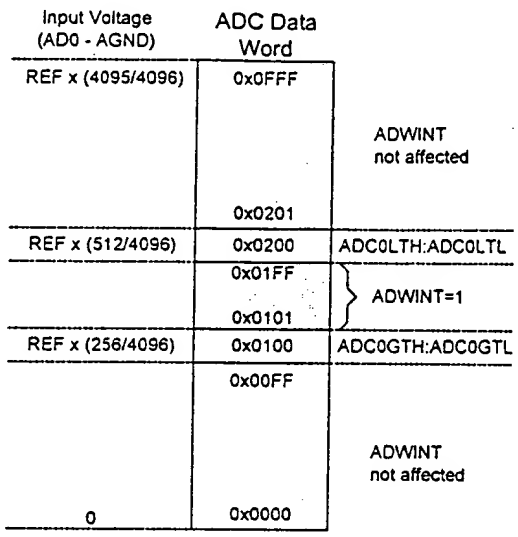
Figure 5-3. Temperature Sensor Transfer Function



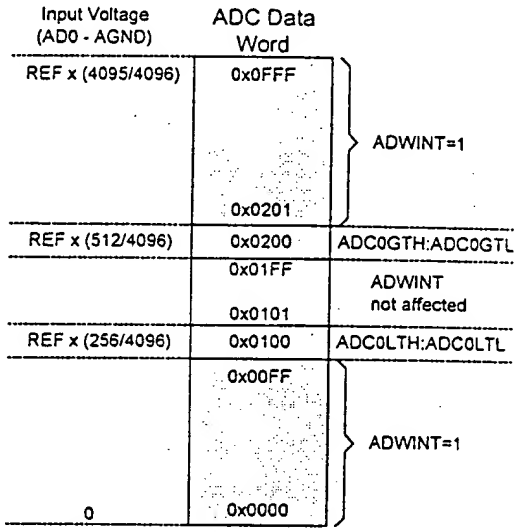
~~#6~~ 13

~~Figure 5.14.~~ ADC Window Interrupt Examples, Right Justified Data



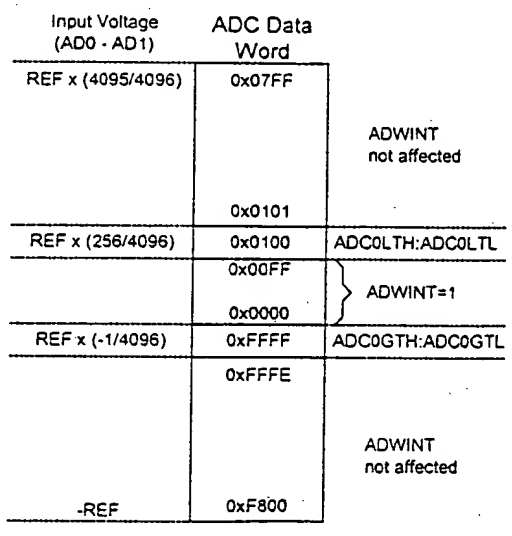
Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0,
ADC0LTH:ADC0LTL = 0x0200,
ADC0GTH:ADC0GTL = 0x0100.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0200 and > 0x0100.



Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0,
ADC0LTH:ADC0LTL = 0x0100,
ADC0GTH:ADC0GTL = 0x0200.

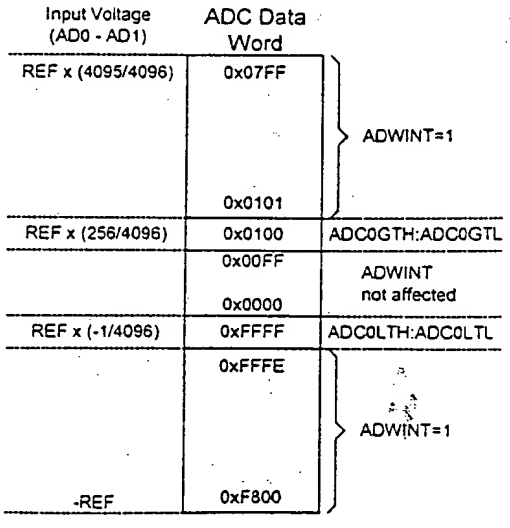
An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 or > 0x0200.



Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 0,
ADC0LTH:ADC0LTL = 0x0100,
ADC0GTH:ADC0GTL = 0xFFFF.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 and > 0xFFFF. (Two's

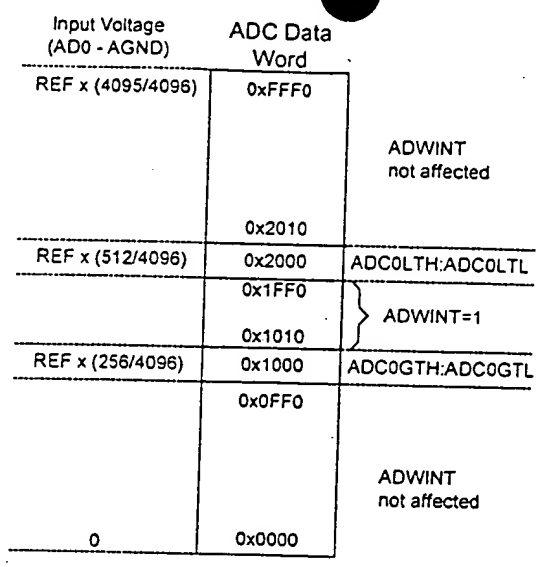


Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 0,
ADC0LTH:ADC0LTH = 0xFFFF,
ADC0GTH:ADC0GTL = 0x0100.

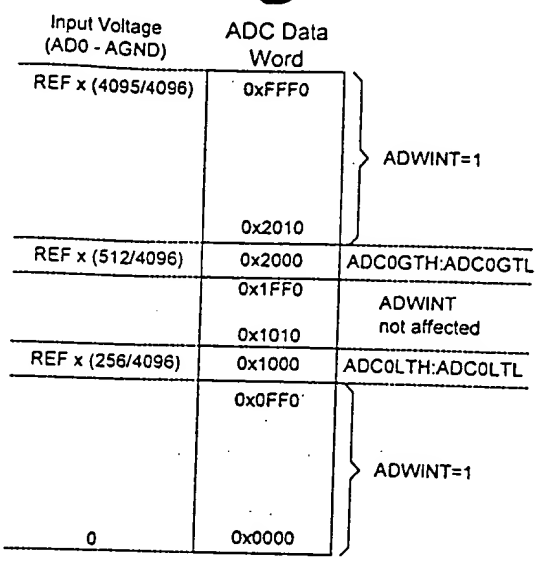
An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFFF or > 0x0100. (Two's Complement

Figure 5.15. ADC Window Interrupt Examples, Left Justified Data



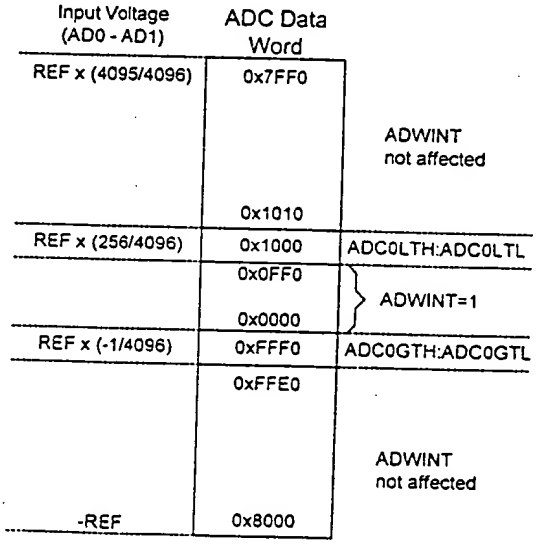
Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x2000,
ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x2000 and > 0x1000.



Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x1000,
ADC0GTH:ADC0GTL = 0x2000.

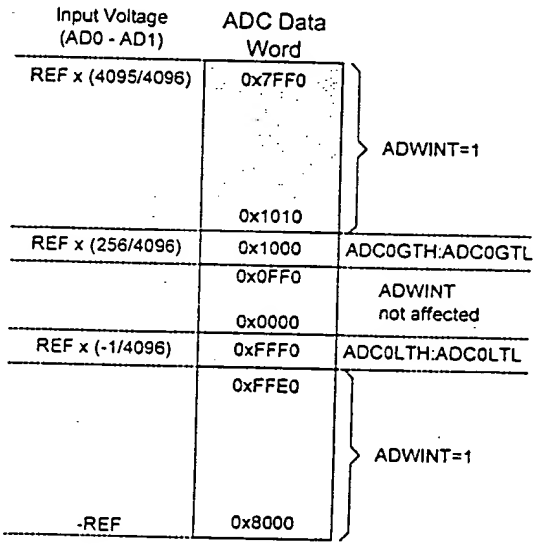
An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 or > 0x2000.



Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x1000,
ADC0GTH:ADC0GTL = 0xFFF0.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 and > 0xFFF0. (Two's Complement math.)



Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,
ADC0LTH:ADC0LTH = 0xFFF0,
ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFF0 or > 0x1000. (Two's Complement math.)

are given in Table 6.1.

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Figure ~~6.1~~. DAC Functional Block Diagram

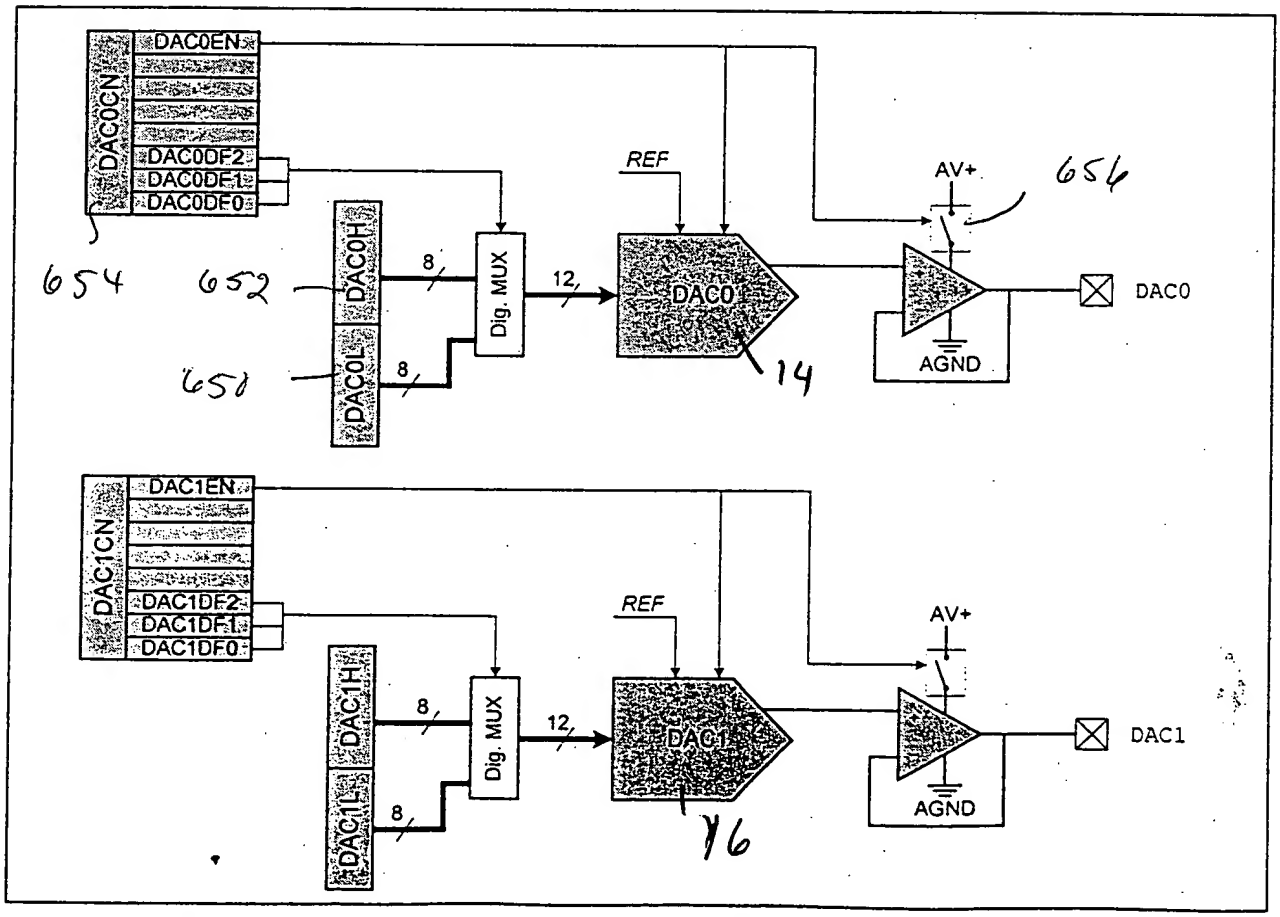
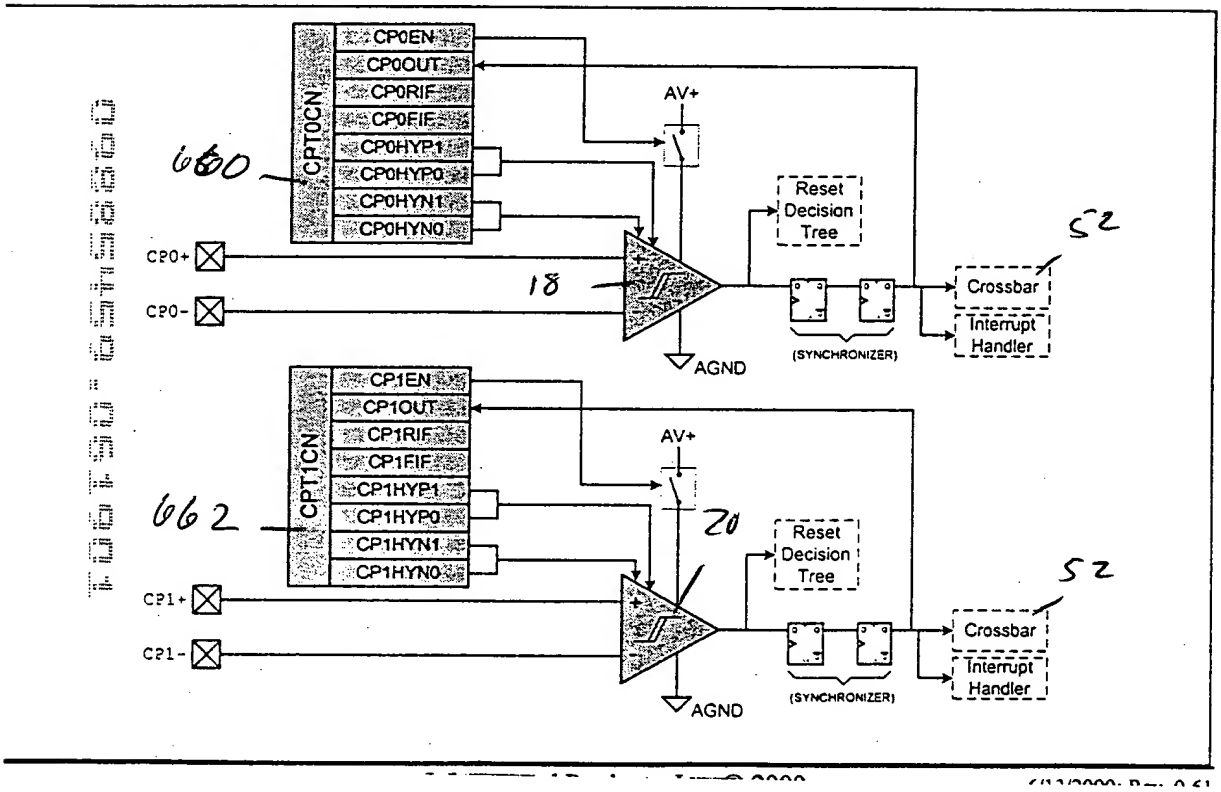


FIG 16

Figure ~~7.1~~. Comparator Functional Block Diagram



~~20~~ 17

Figure ~~7.2~~. Comparator Hysteresis Plot

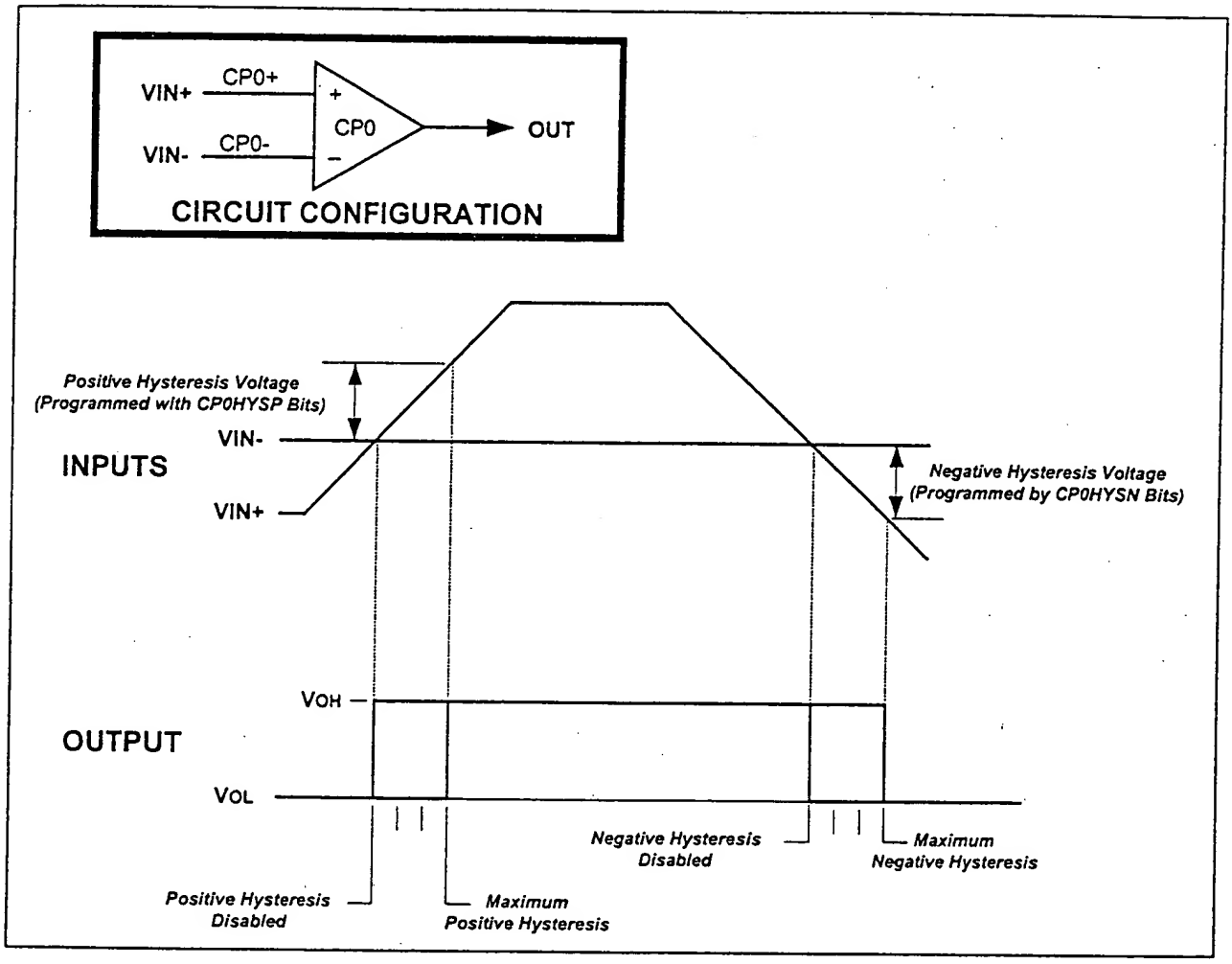
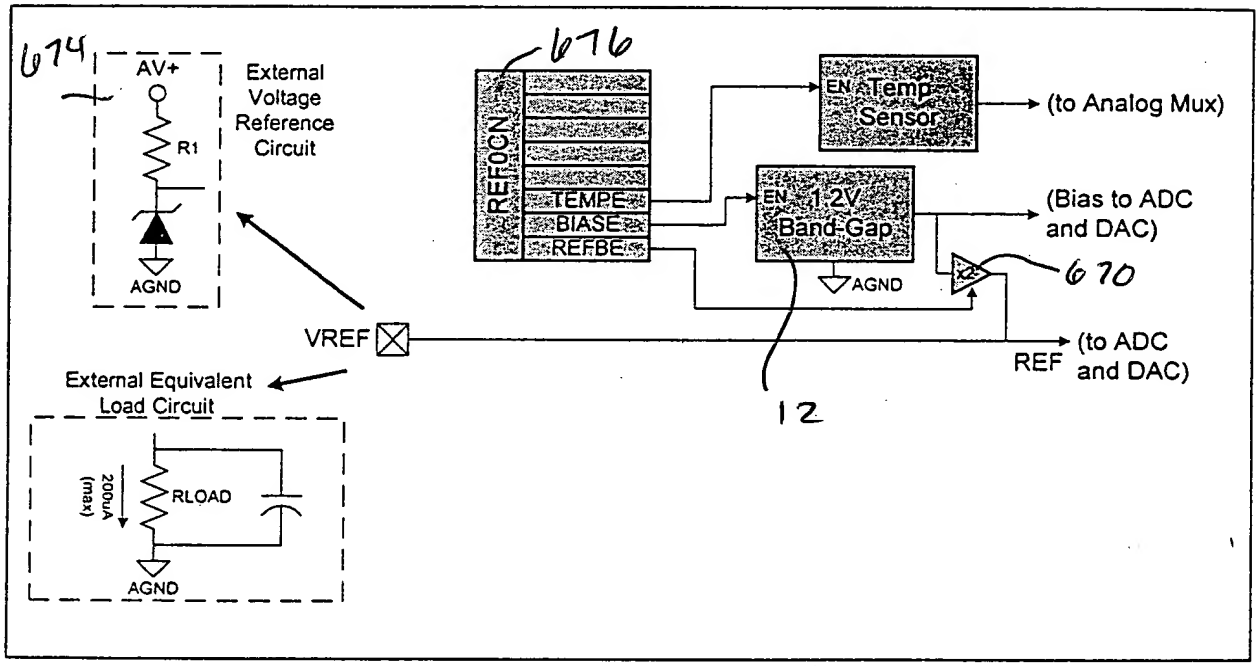


Figure 8.1. Voltage Reference Functional Block Diagram



~~22~~ 19

Figure ~~9~~.1. CIP-51 Block Diagram

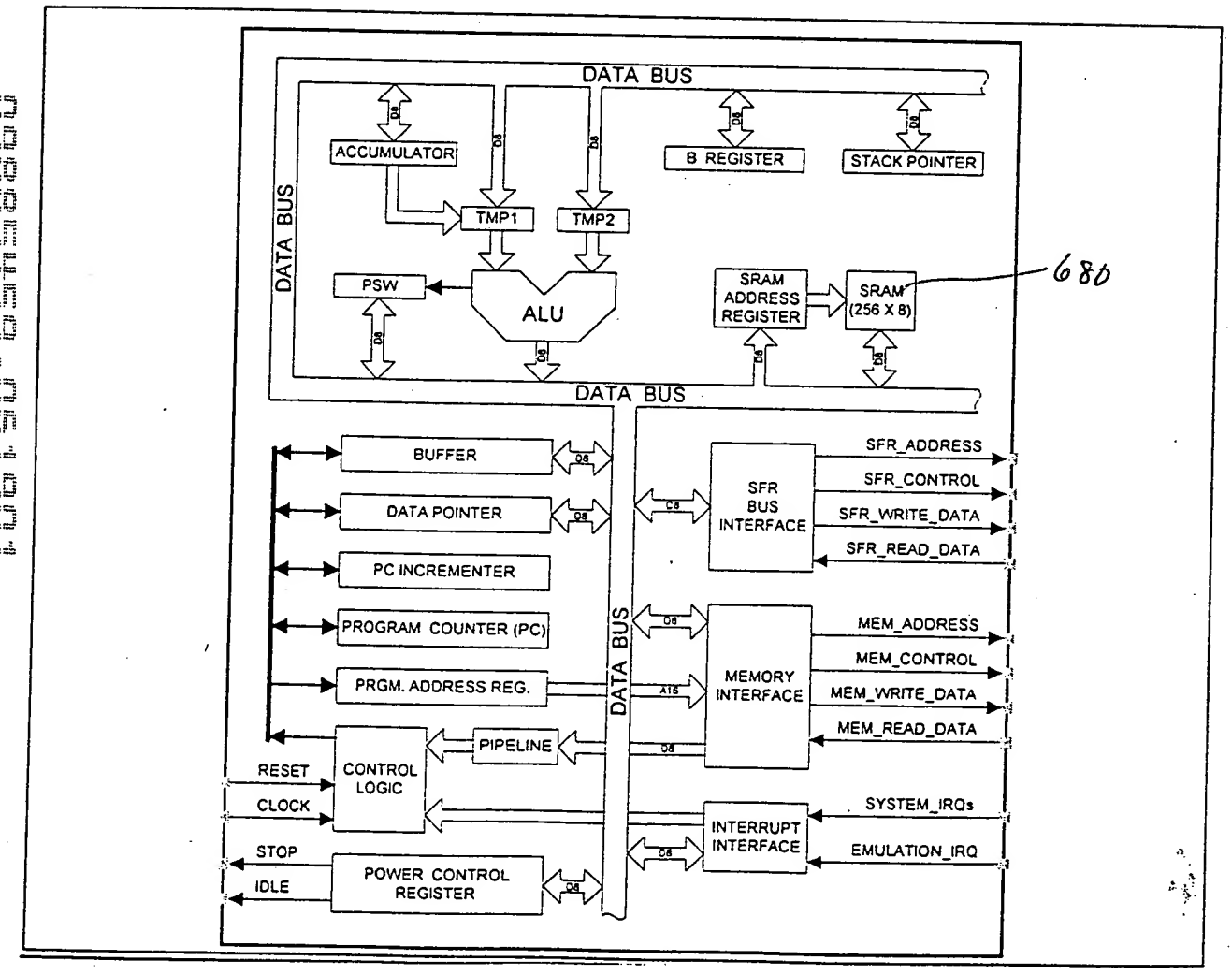


Figure ~~9.2~~ 20. Memory Map

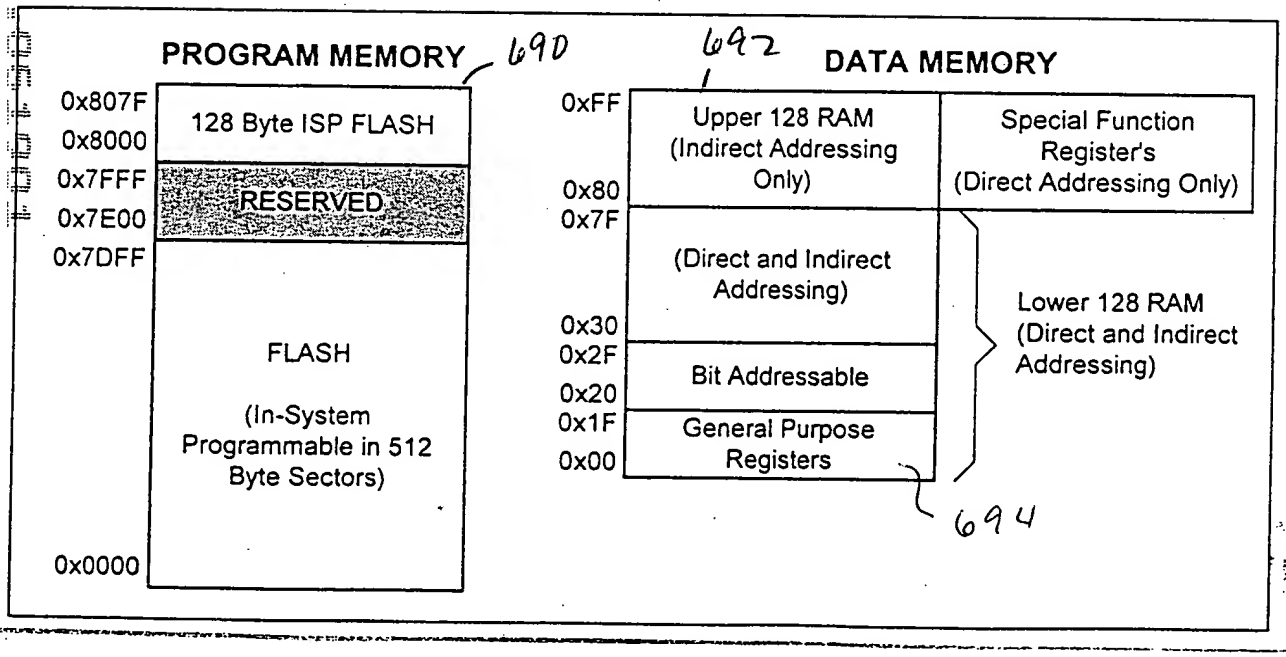


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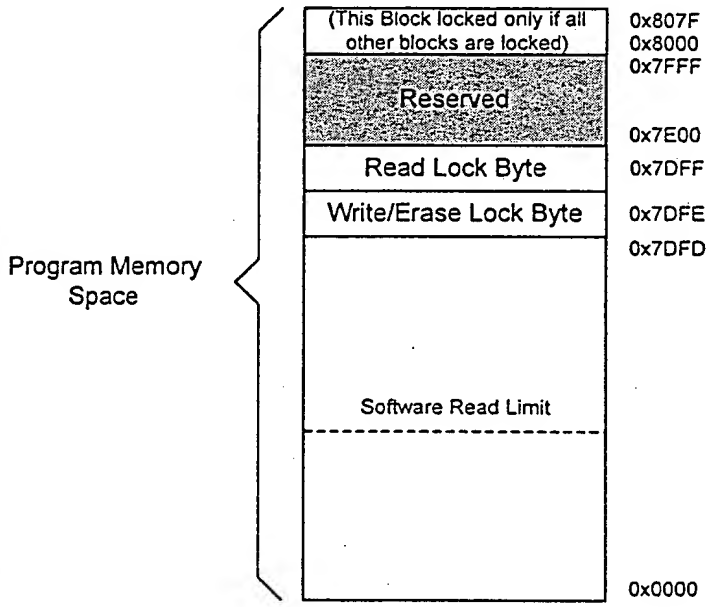
FIGURE 21

~~Figure 10.1.~~ Flash Program Memory Security Bytes



Read and Write/Erase Security Bits. (Bit 7 is MSB.)

Bit	Memory Block
7	0x7000 - 0x7DFD
6	0x6000 - 0x6FFF
5	0x5000 - 0x5FFF
4	0x4000 - 0x4FFF
3	0x3000 - 0x3FFF
2	0x2000 - 0x2FFF
1	0x1000 - 0x1FFF
0	0x0000 - 0x0FFF

FLASH Read Lock Byte

Bits7-0: Each bit locks a corresponding block of memory. (Bit 7 is MSB.)

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

FLASH Write/Erase Lock Byte

Bits7-0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

FLASH Access Limit Register (FLACL)

The content of this register is used as the high byte of the 16-bit software read limit address. The 16-bit read limit address value is calculated as 0xNN00 where NN is replaced by content of this register on reset. Software running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase, locations below this address. Any attempts to read locations below this limit will return the value 0x00.

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Figure ~~11.2~~. VDD Monitor Timing Diagram

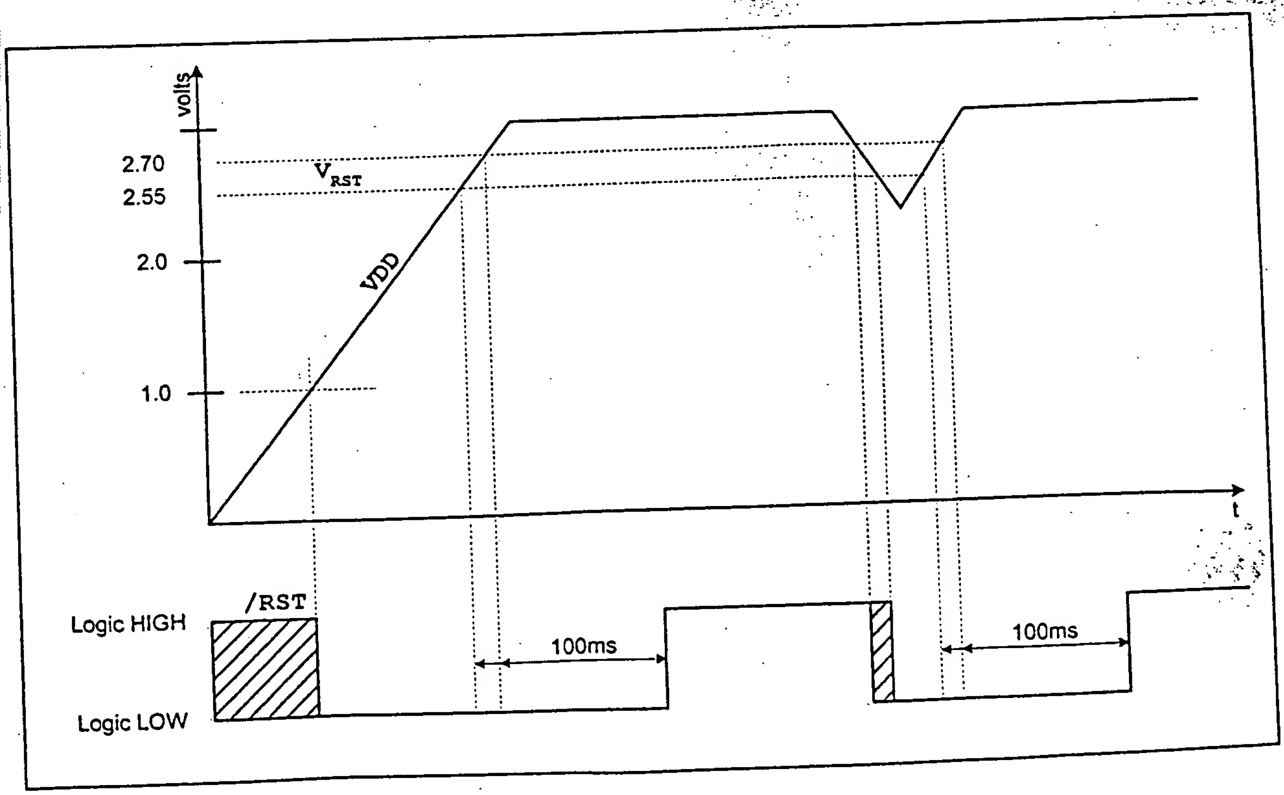

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Figure 12.1. Oscillator Diagram

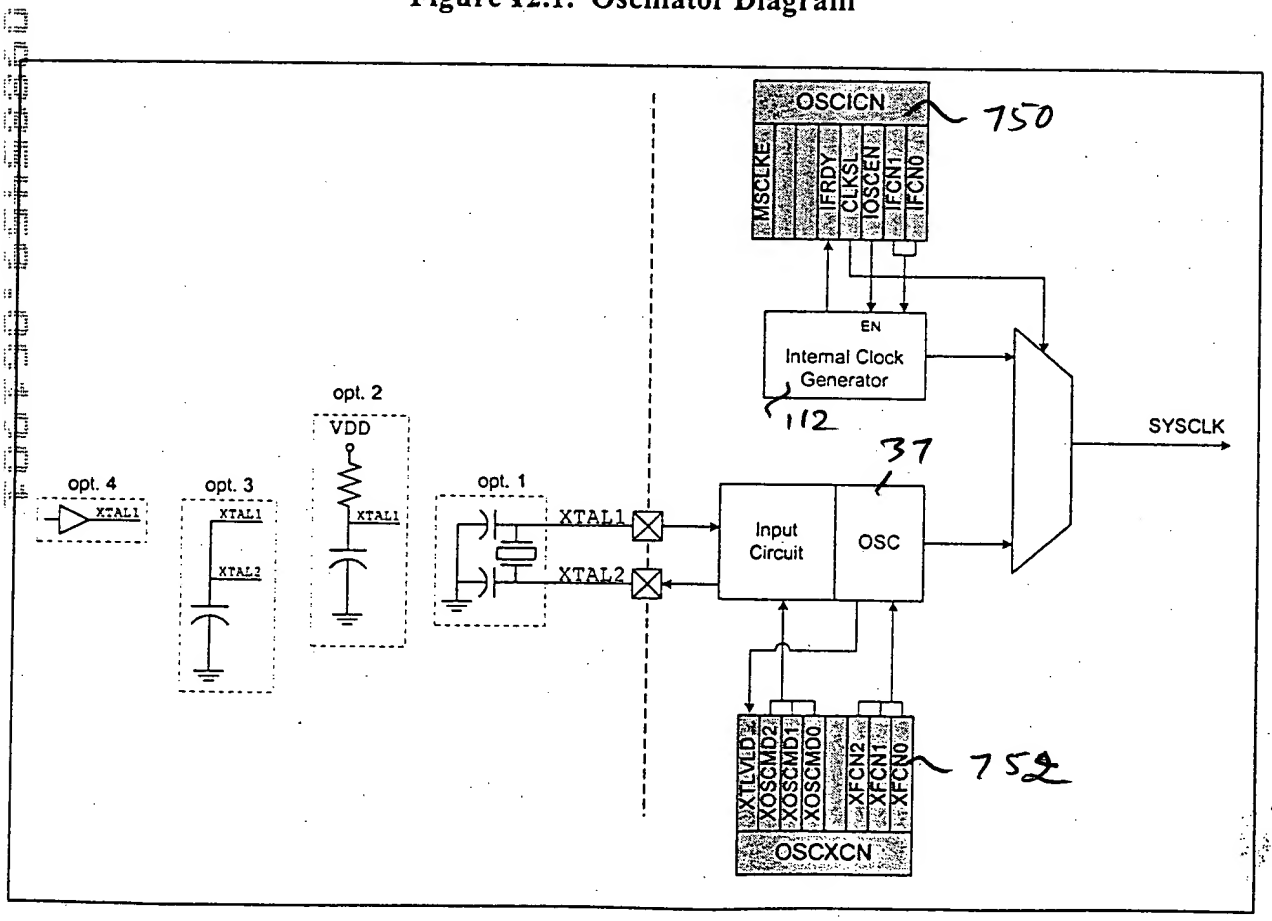

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Figure ~~13.2~~. Port I/O Cell Block Diagram

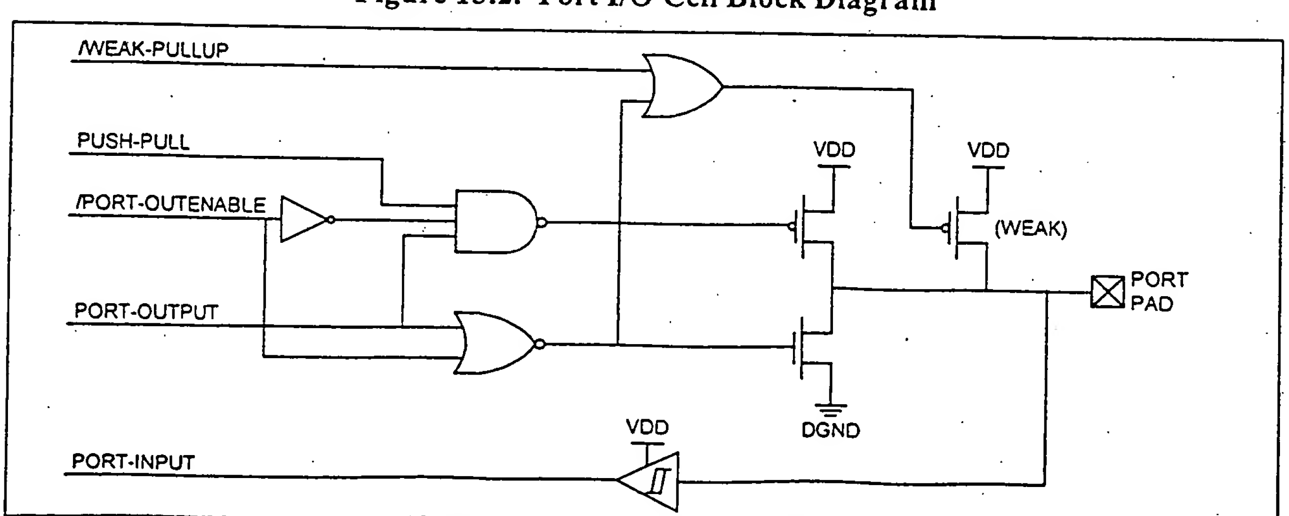

Figure 14.1. SMBus Block Diagram

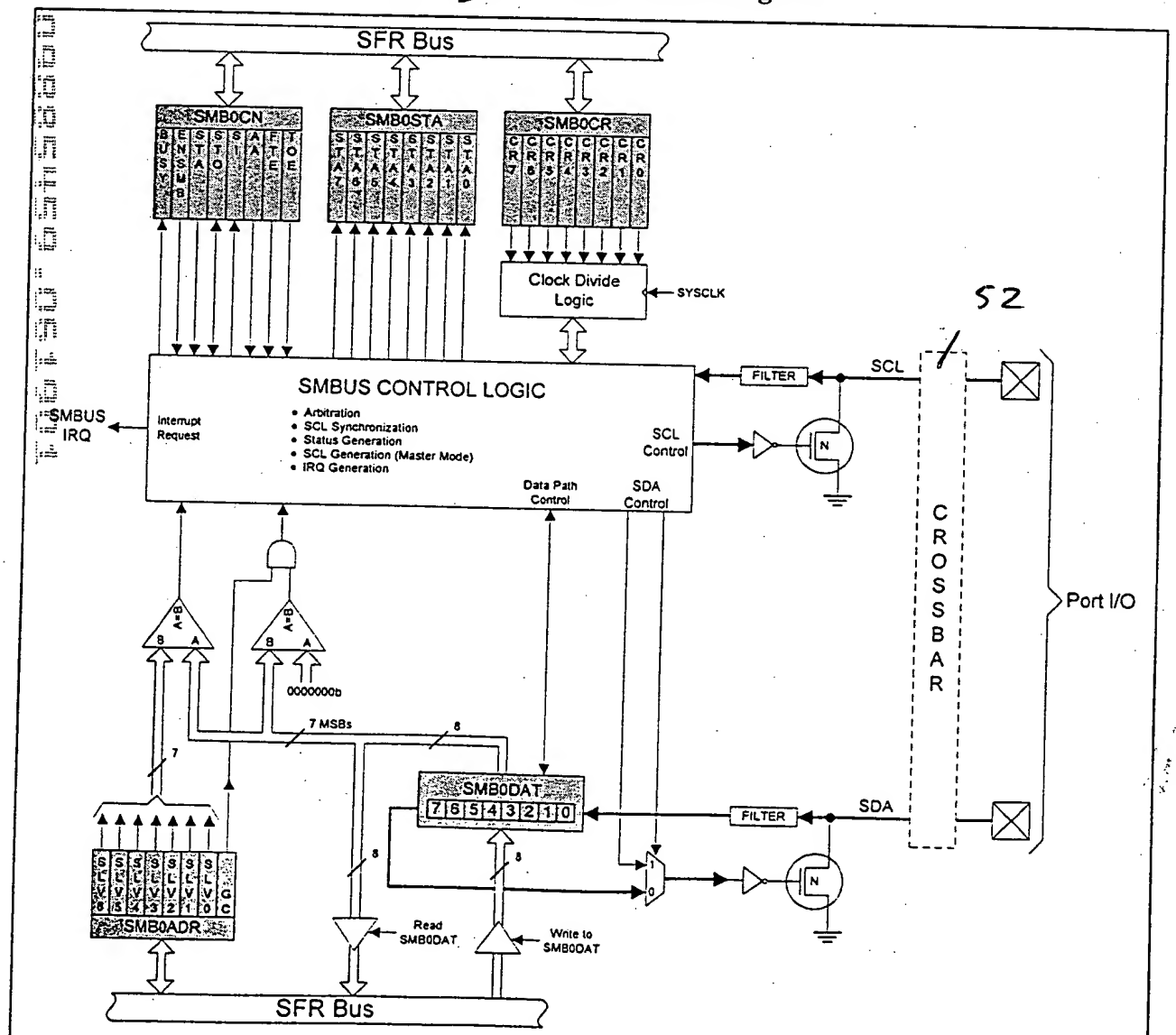

Figure 14.2. Typical SMBus Configuration

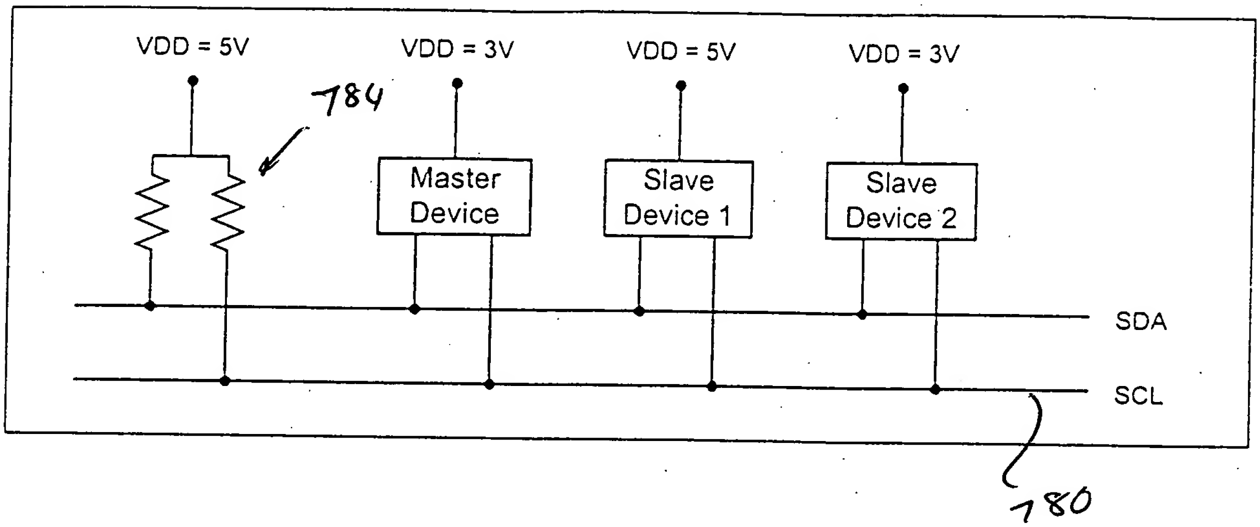

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Figure 14.3. SMBus Transaction

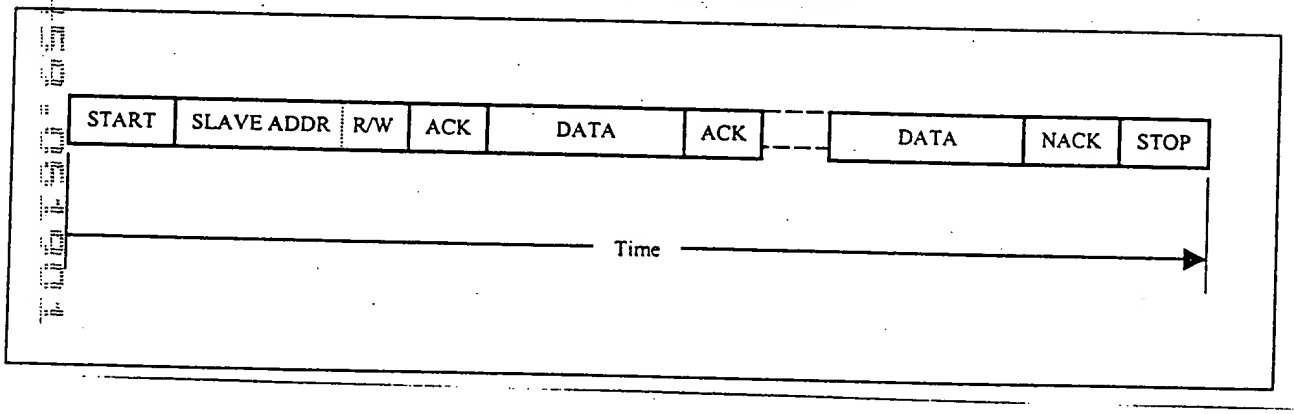

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Figure 15.1. SPI Block Diagram

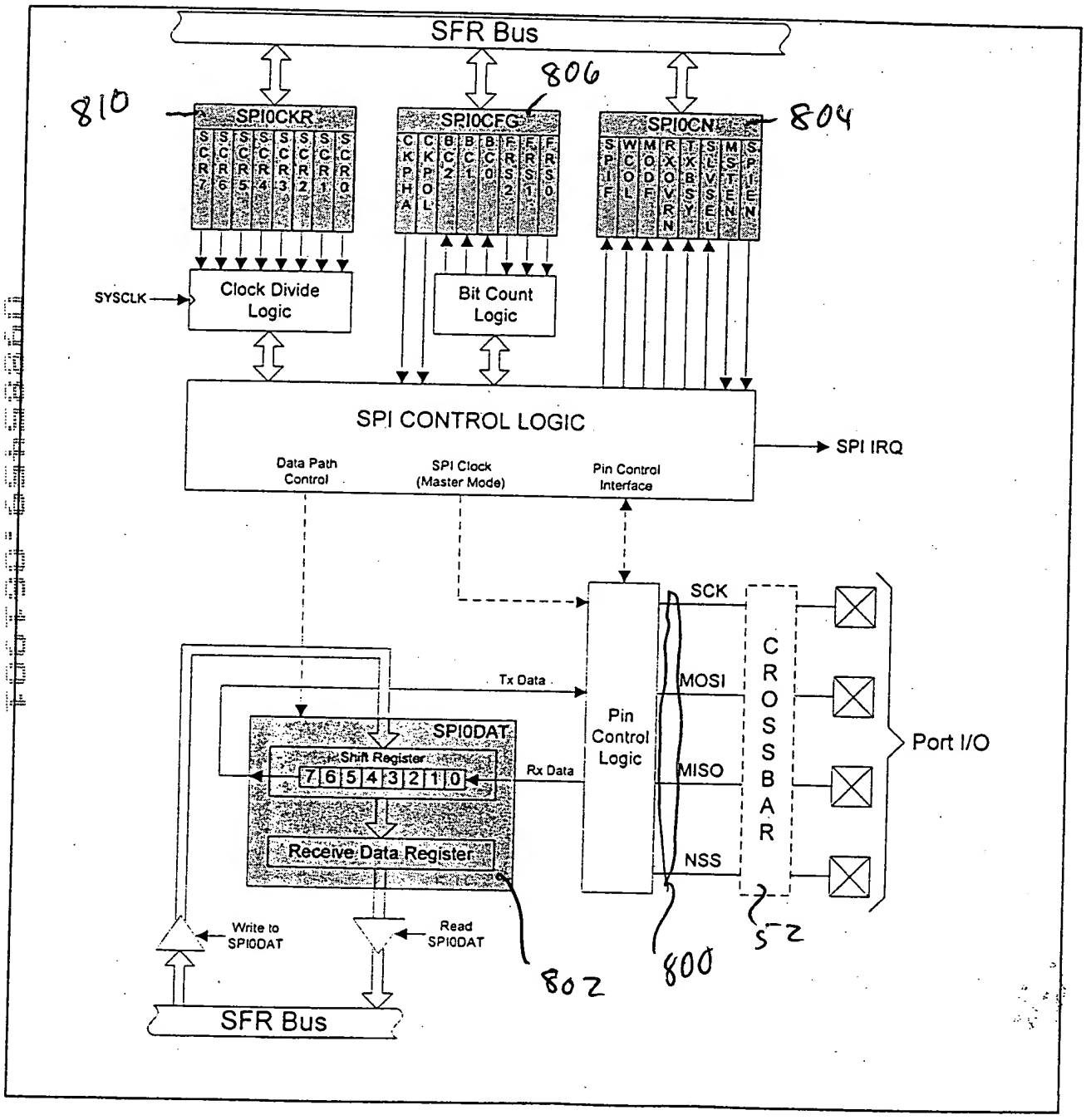

Figure 15.2. Typical SPI Interconnection

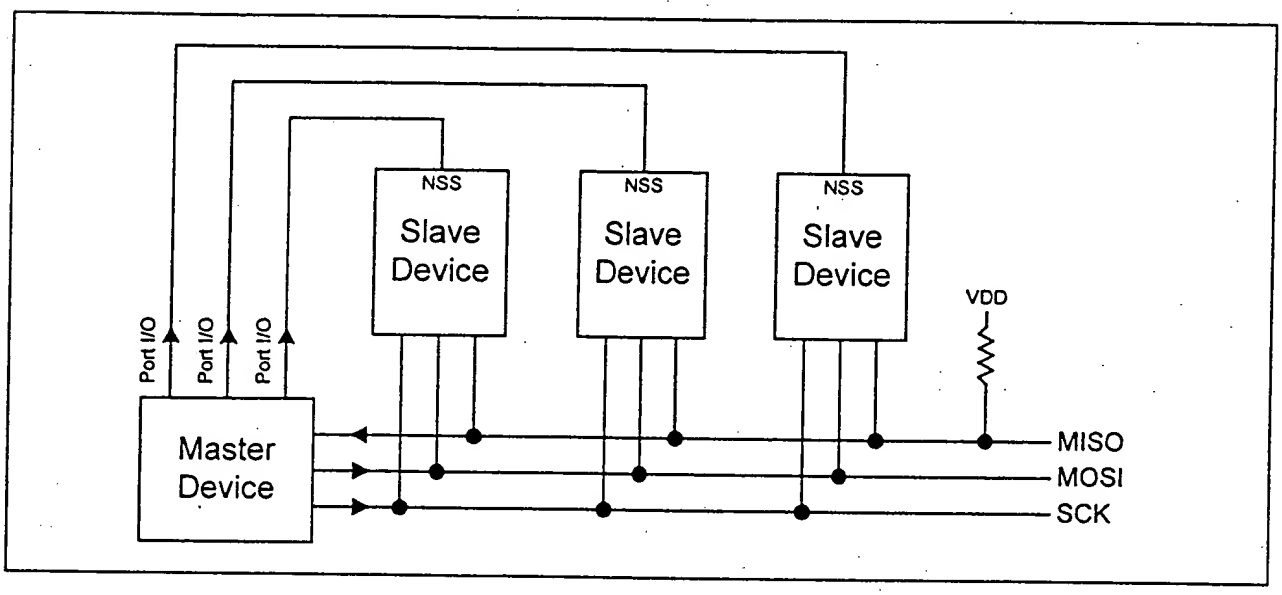

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Figure 15.3. Full Duplex Operation

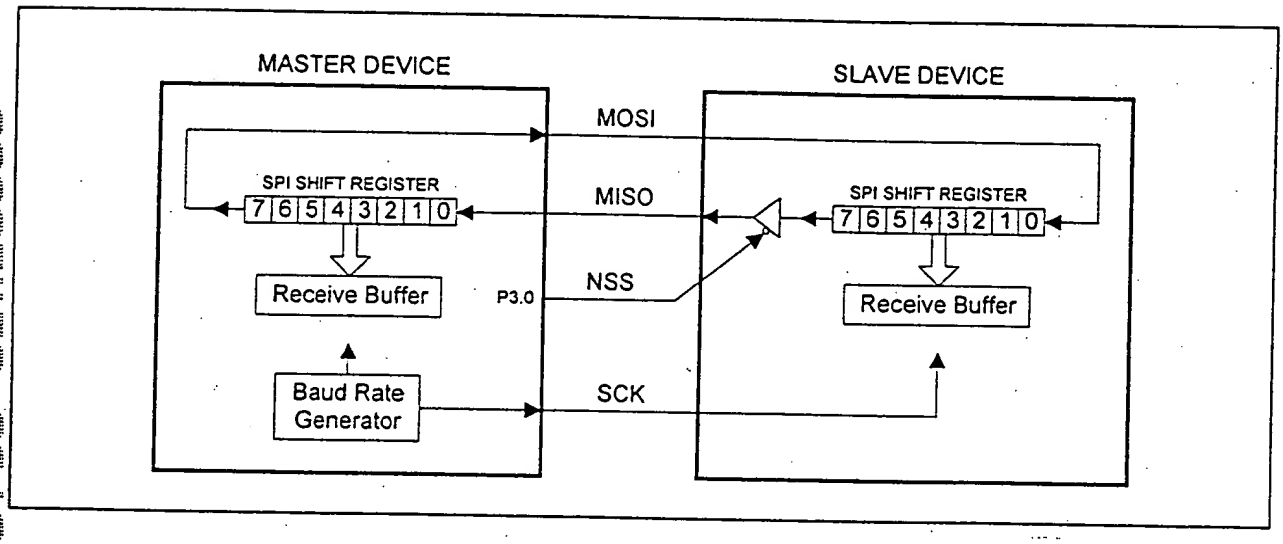

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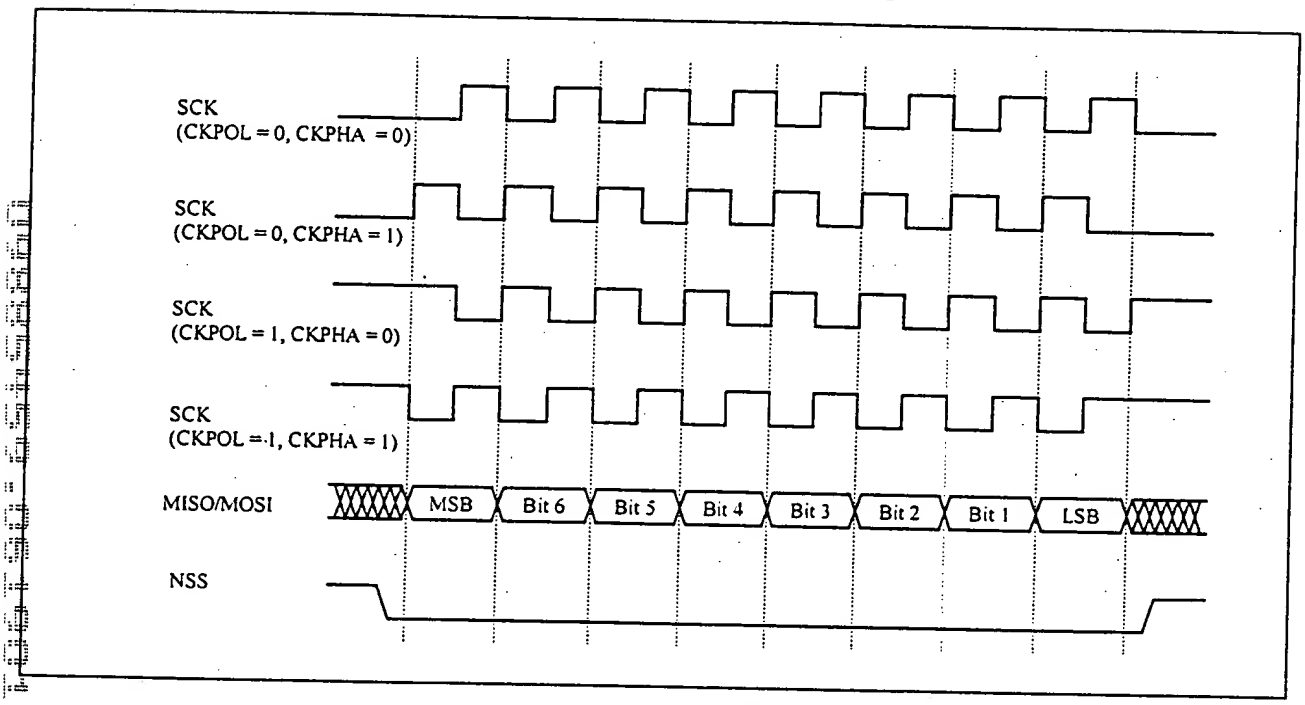
Figure ~~15~~.4. Data/Clock Timing Diagram



820

FIG 3B

Figure 16.1. UART Block Diagram

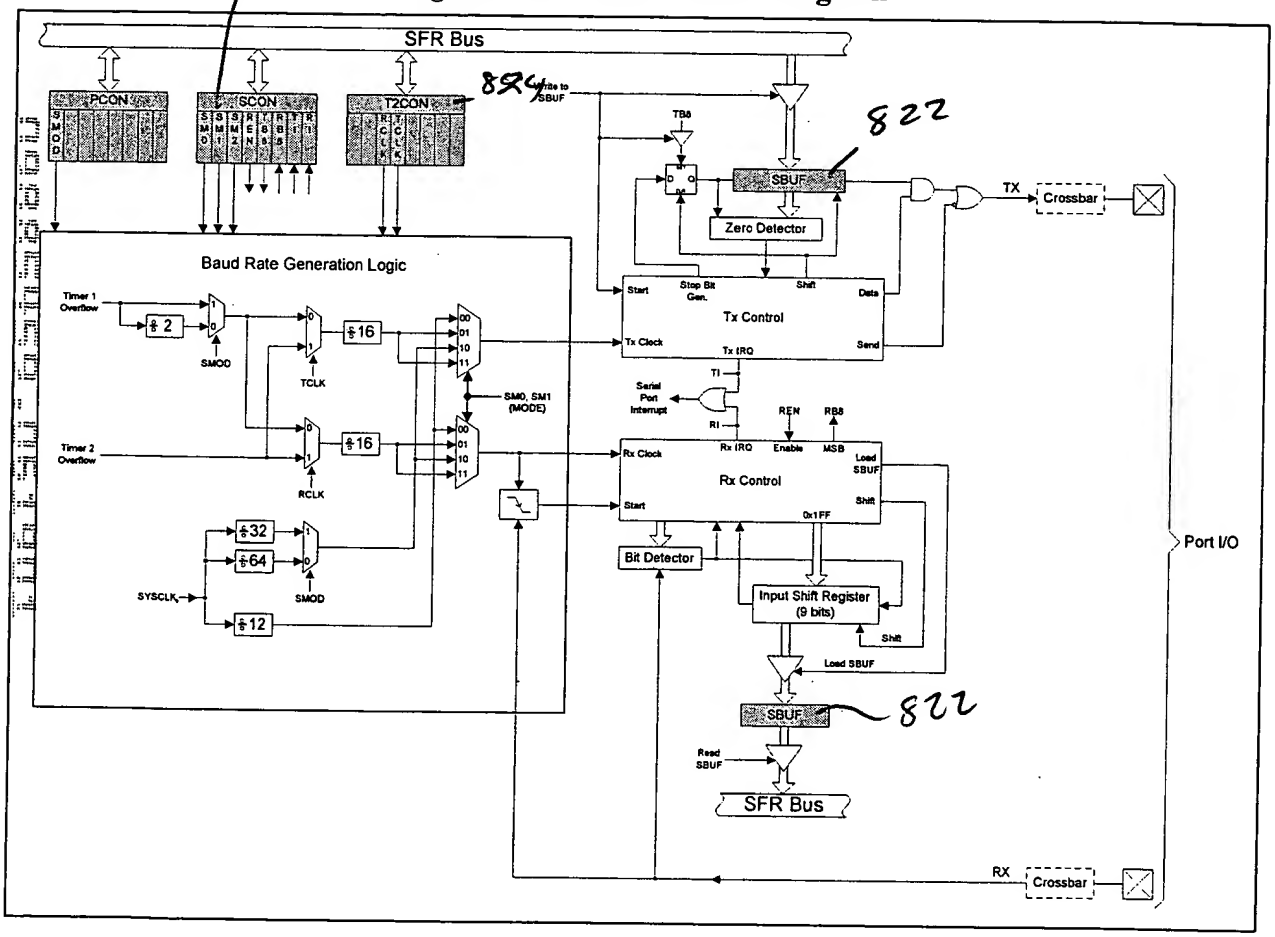


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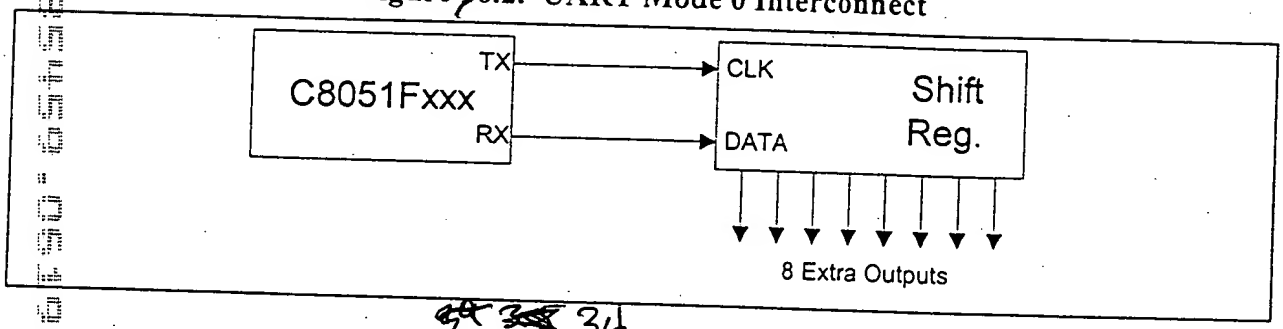
Figure 16.2. UART Mode 0 Interconnect



34

Figure 16.3. UART Mode 0 Timing Diagram

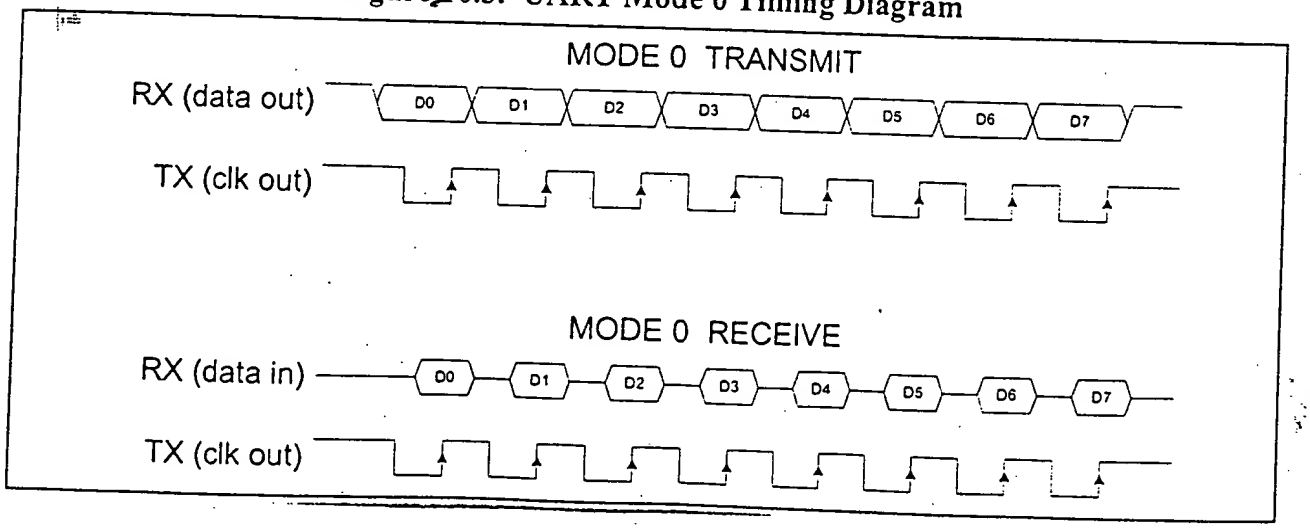


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Figure 16.4. UART Mode 1 Timing Diagram

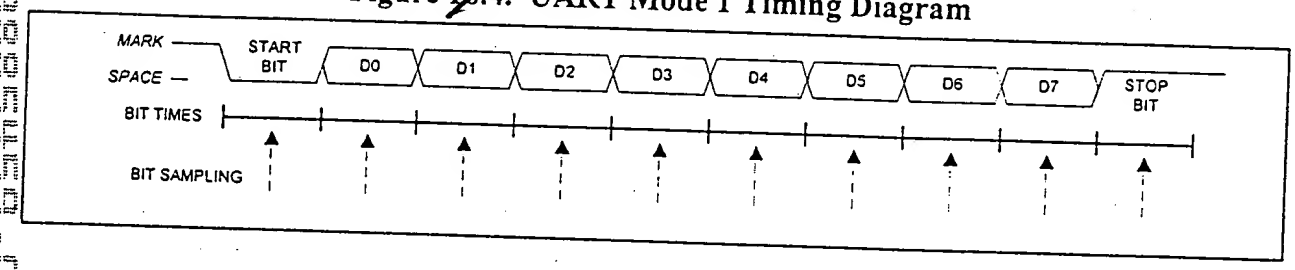

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Figure 16.5. UART Modes 1, 2, and 3 Interconnect Diagram

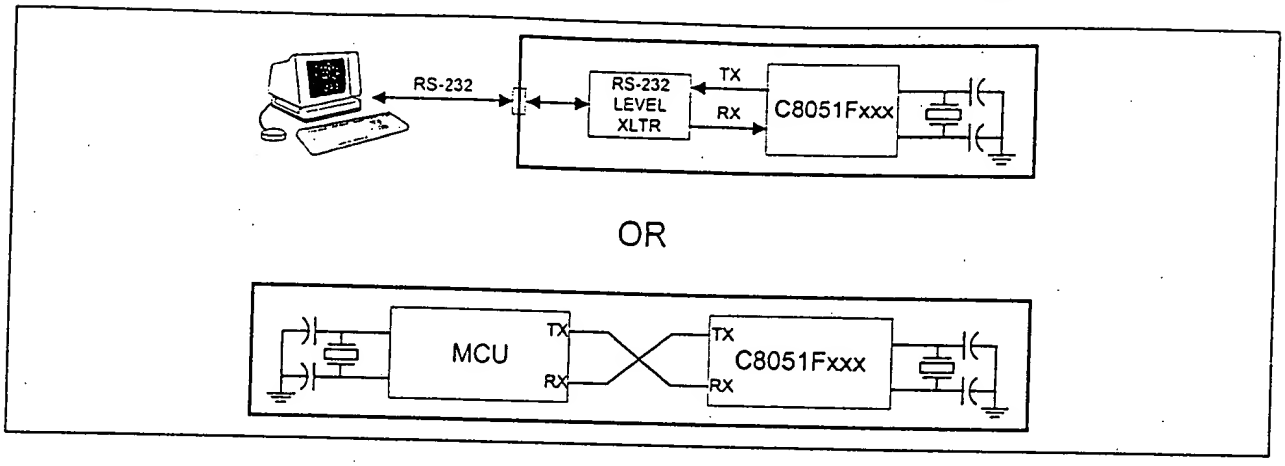

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Figure 16.6. UART Modes 2 and 3 Timing Diagram

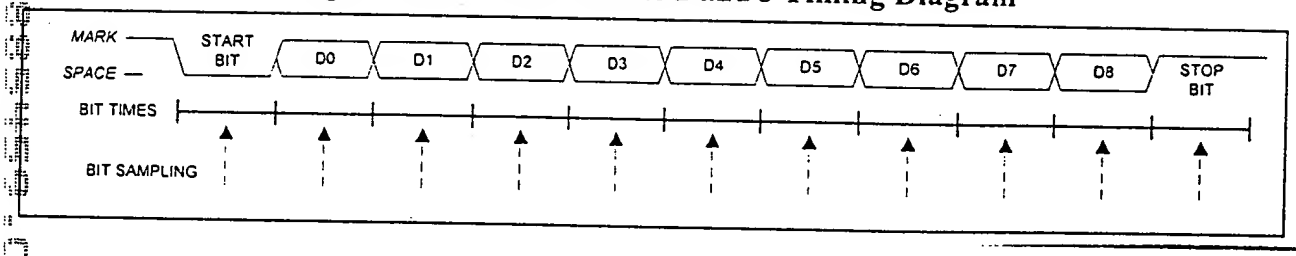

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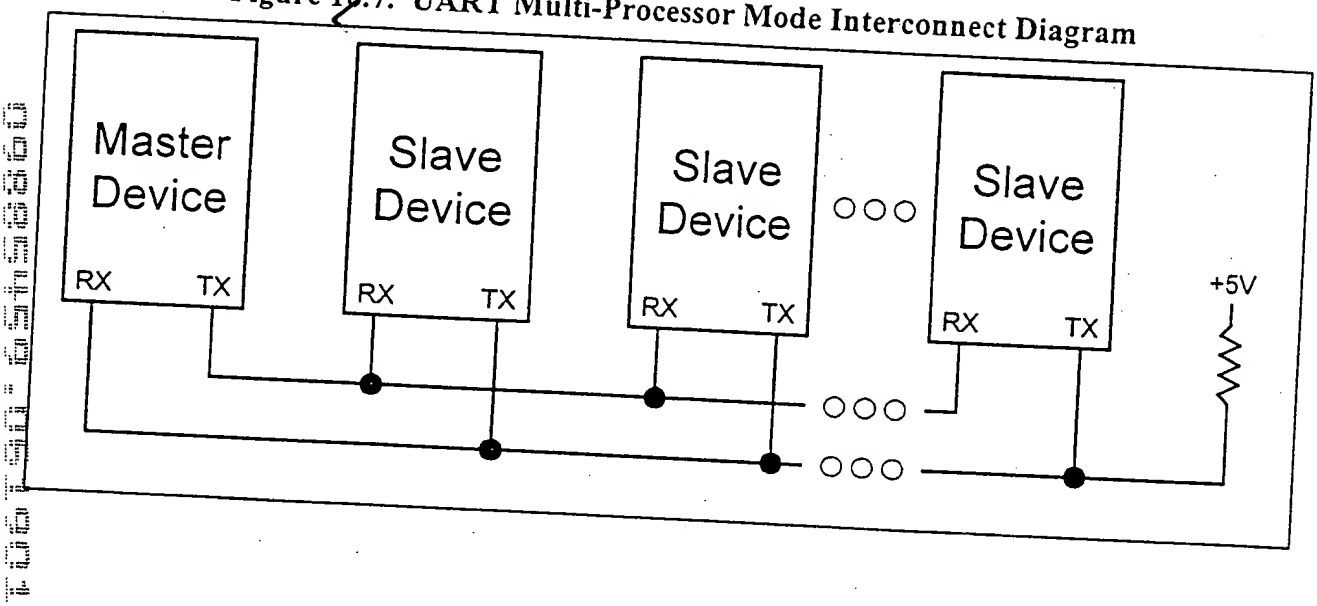
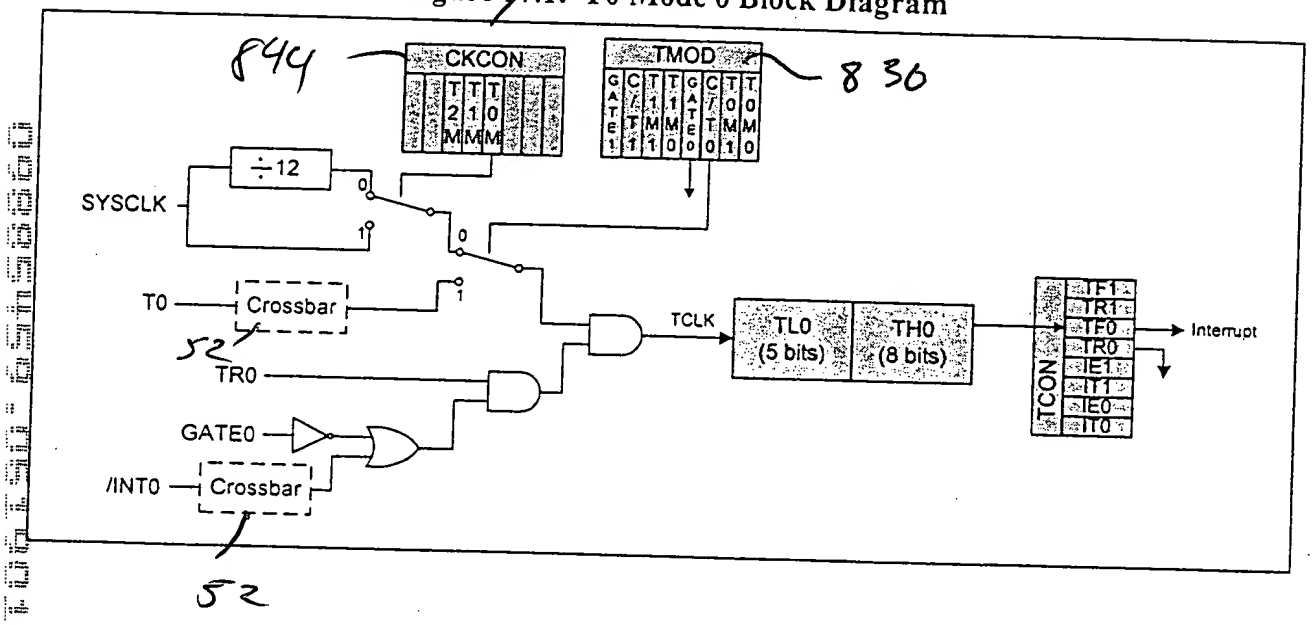
Figure 16.7. UART Multi-Processor Mode Interconnect Diagram



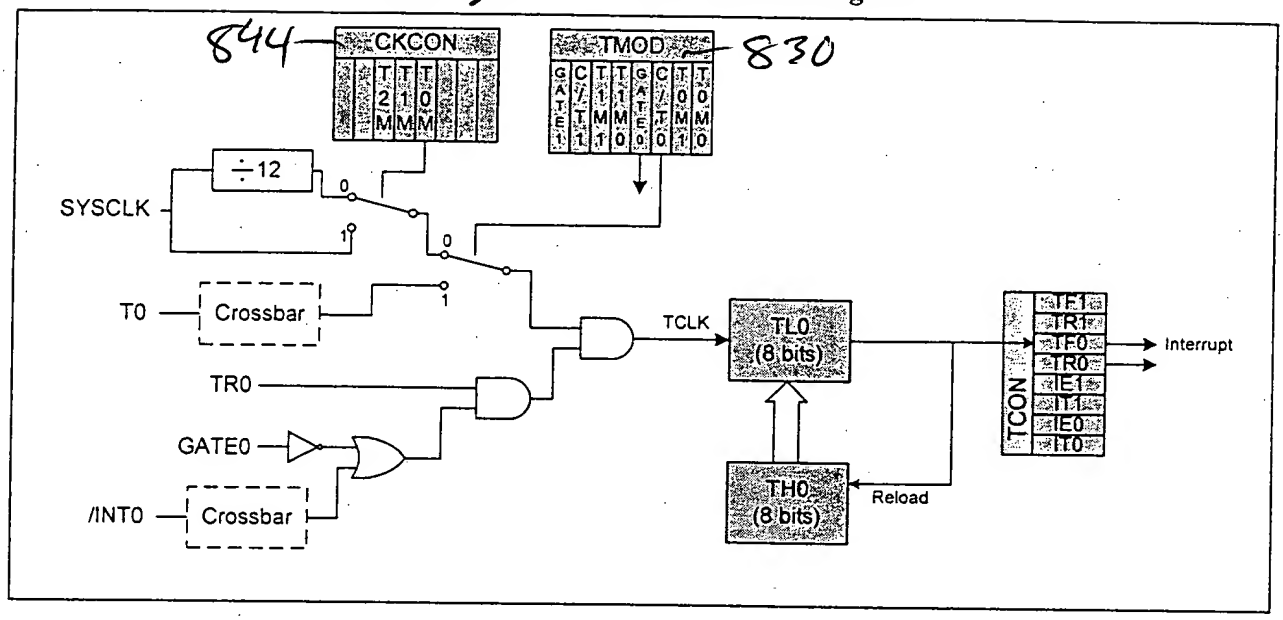
39
44

Figure 17.1. T0 Mode 0 Block Diagram



40

Figure 17.2. T0 Mode 2 Block Diagram



41

Figure 17.3. T0 Mode 3 Block Diagram

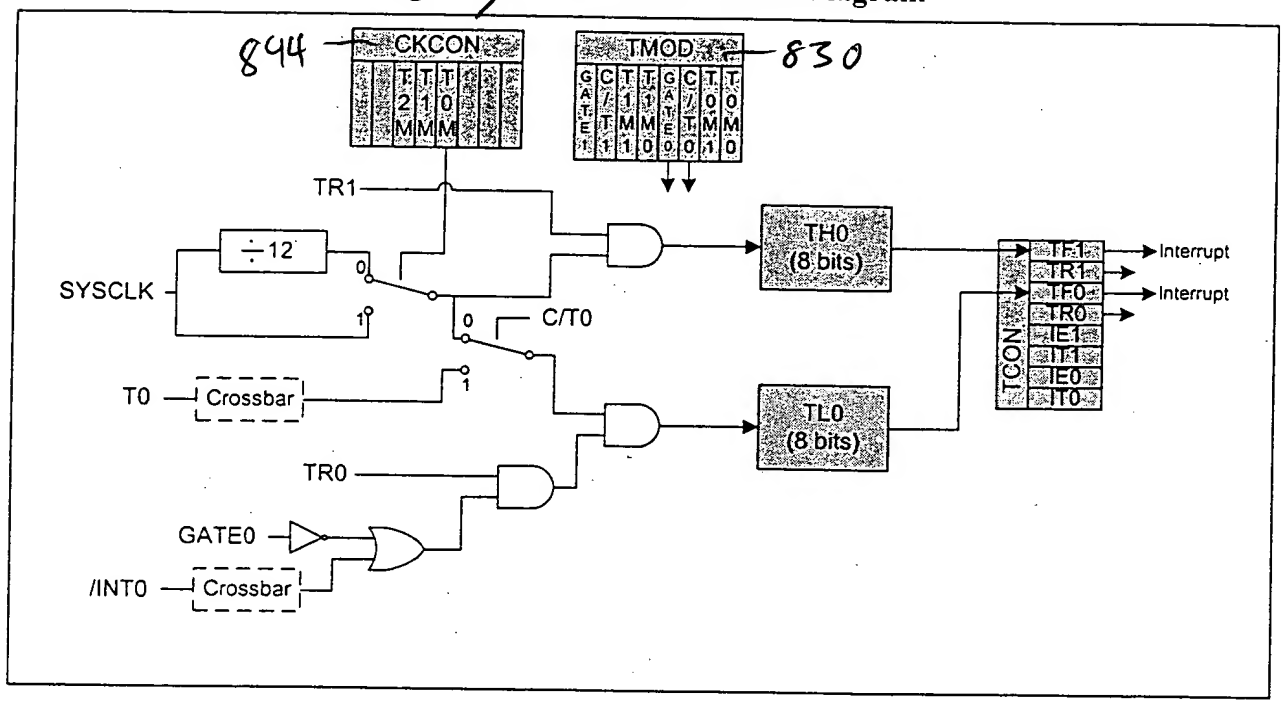


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Figure 17.11. T2 Mode 0 Block Diagram

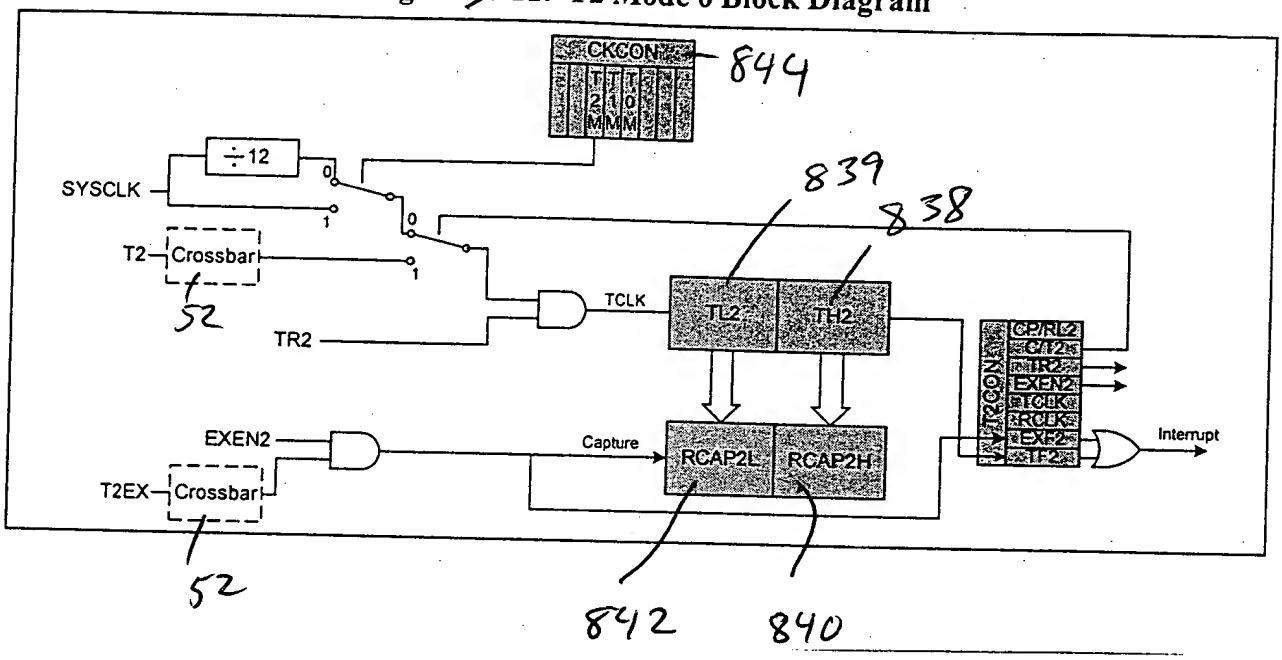

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Figure 17.12. T2 Mode 1 Block Diagram

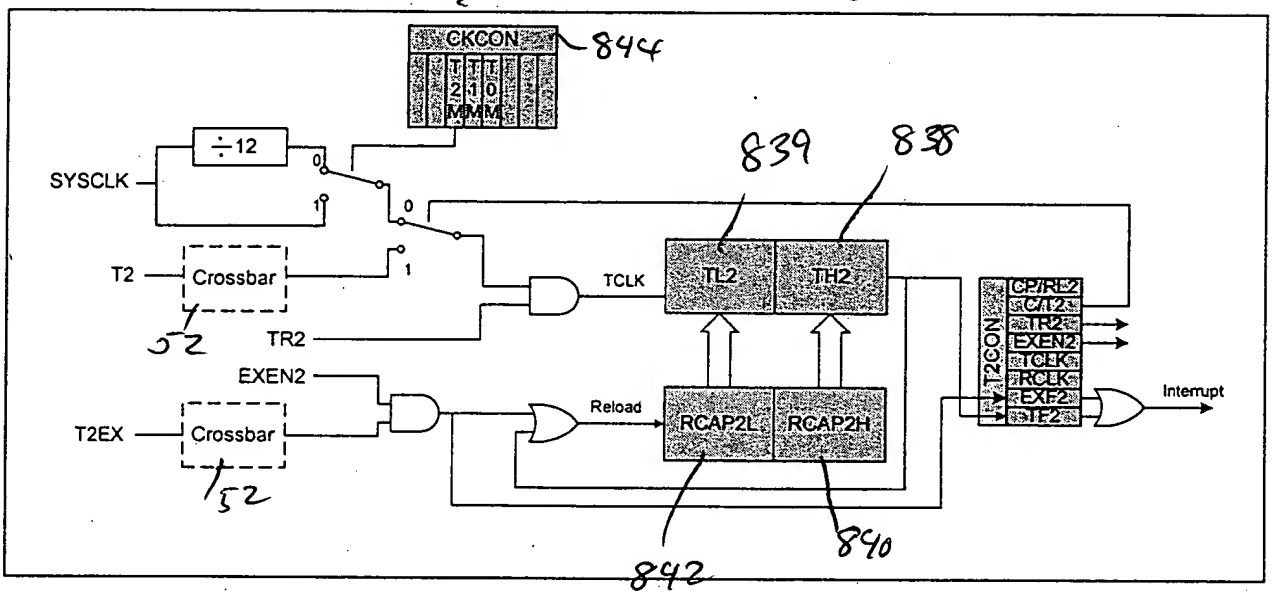
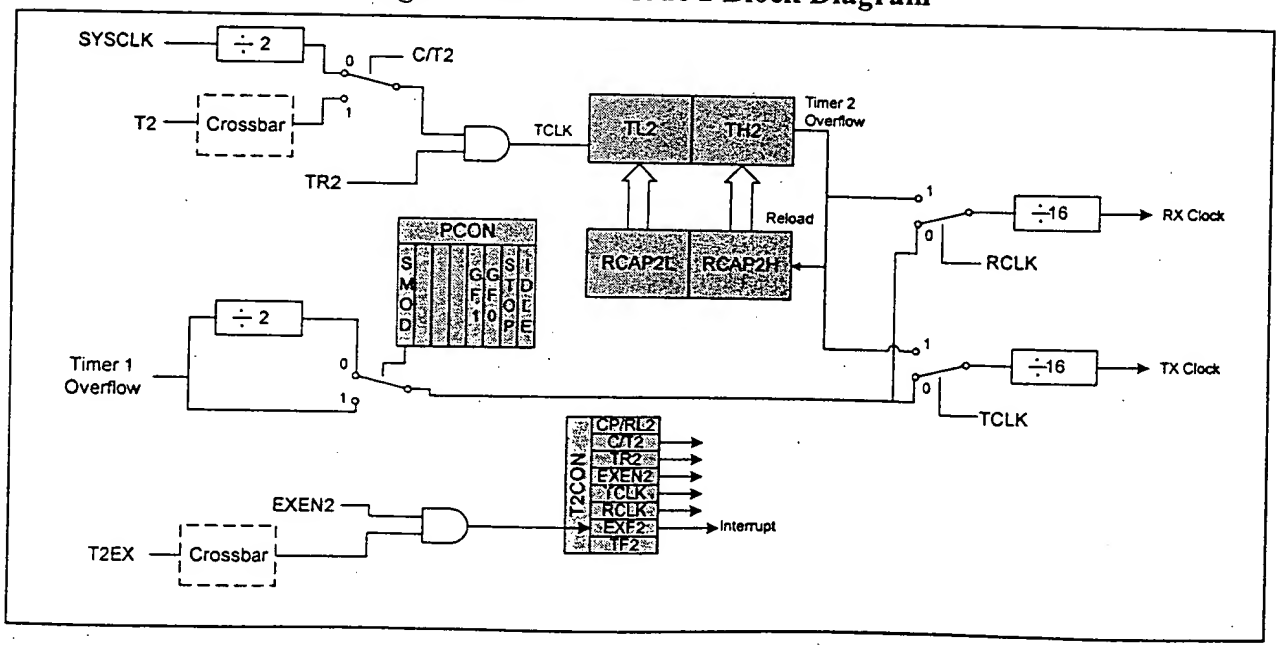
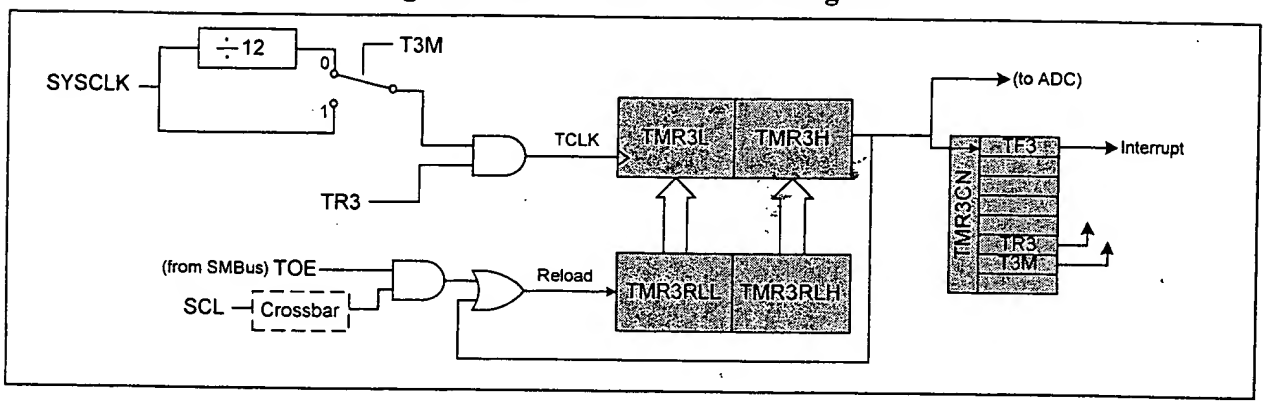


Figure ~~17.13~~. T2 Mode 2 Block Diagram



45

Figure ~~17.19~~. Timer 3 Block Diagram



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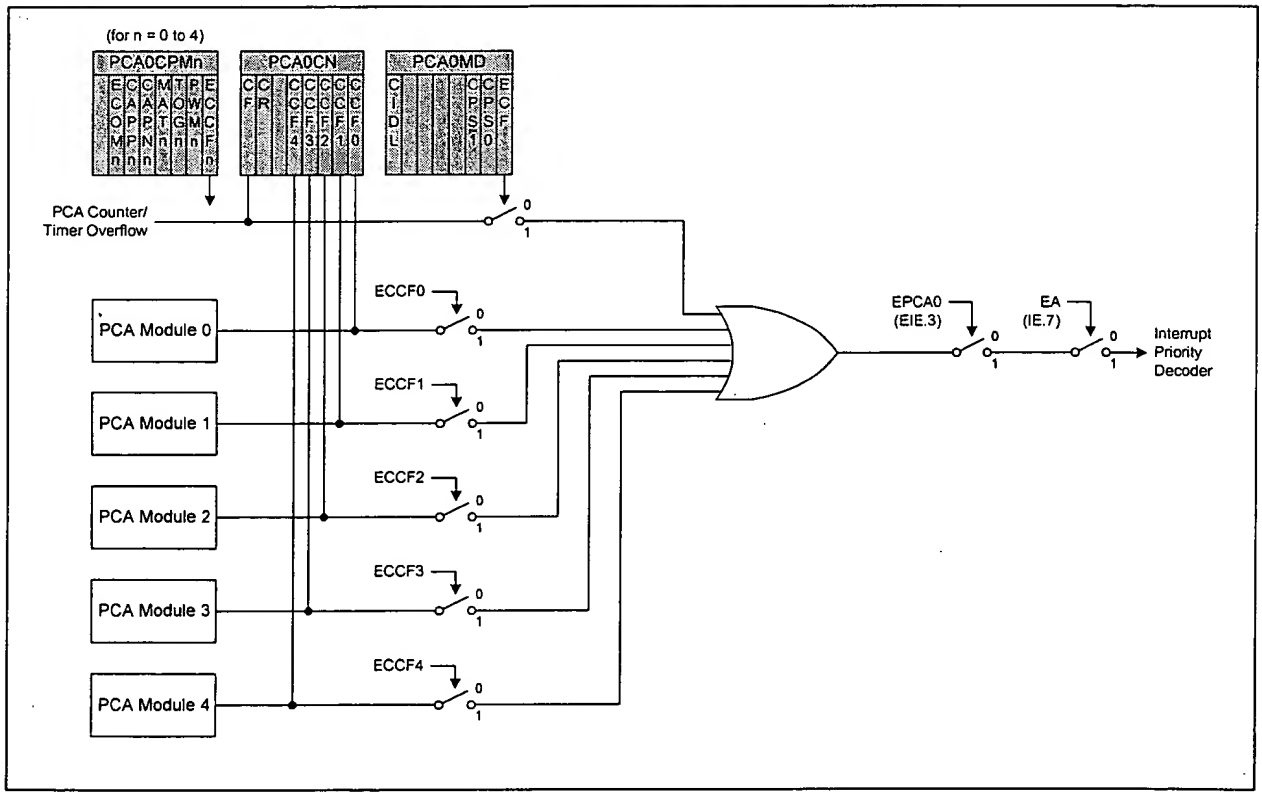

CCDA 25,768
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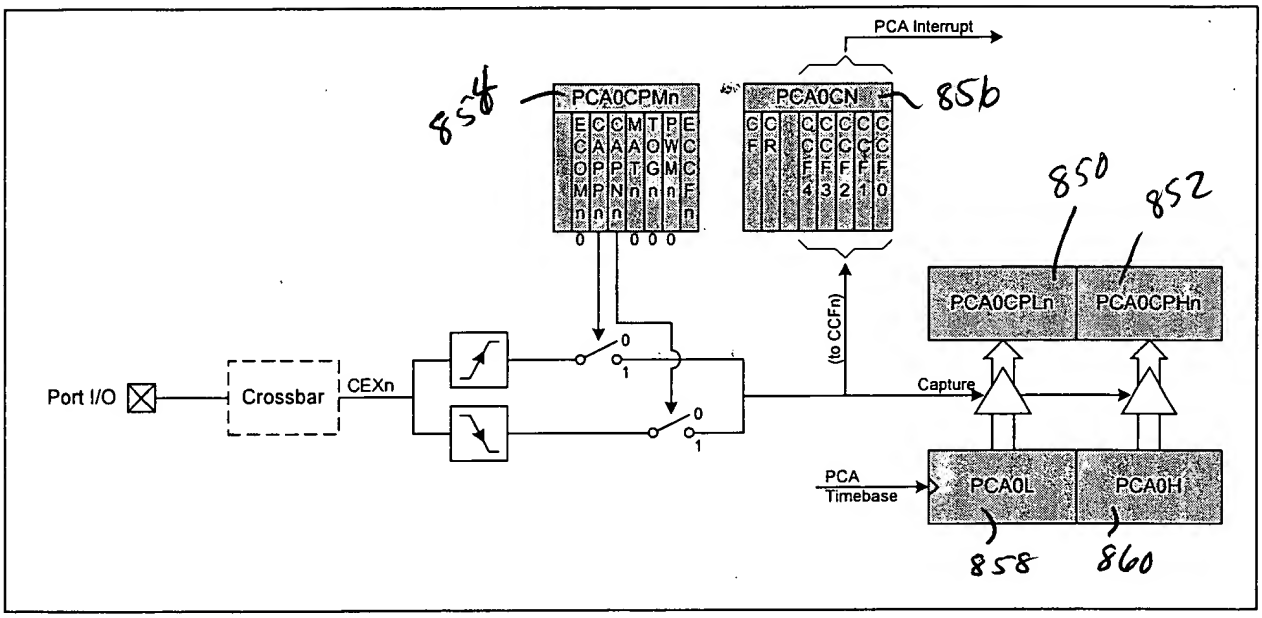
Figure ~~18.~~3. PCA Capture Mode Diagram



48

Figure ~~18.4.~~ PCA Software Timer Mode Diagram

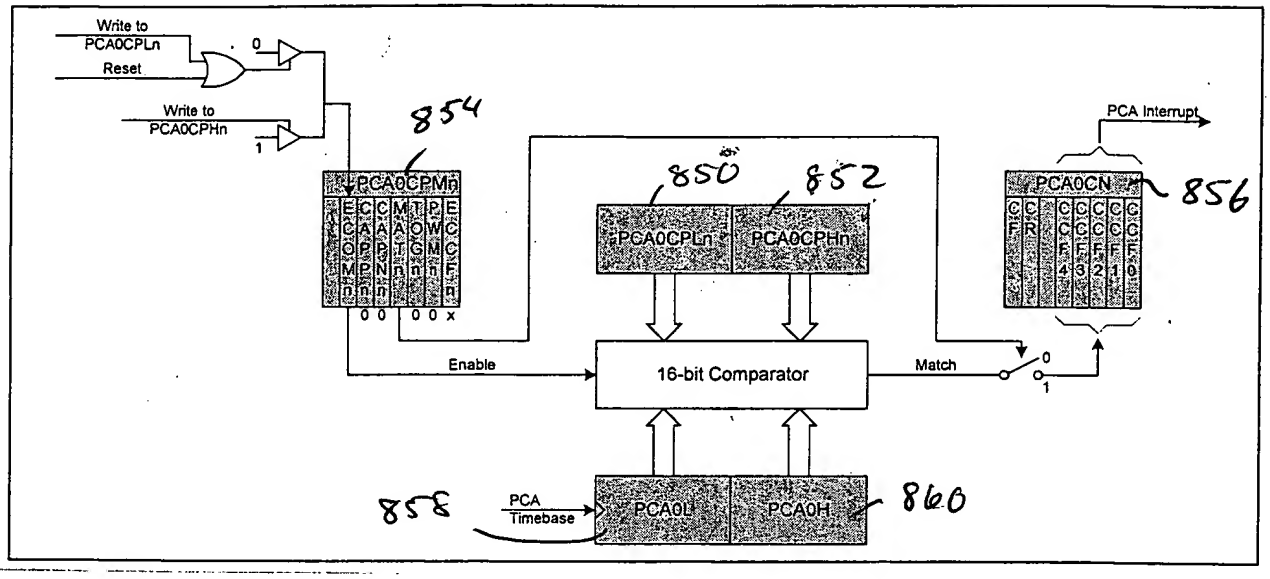
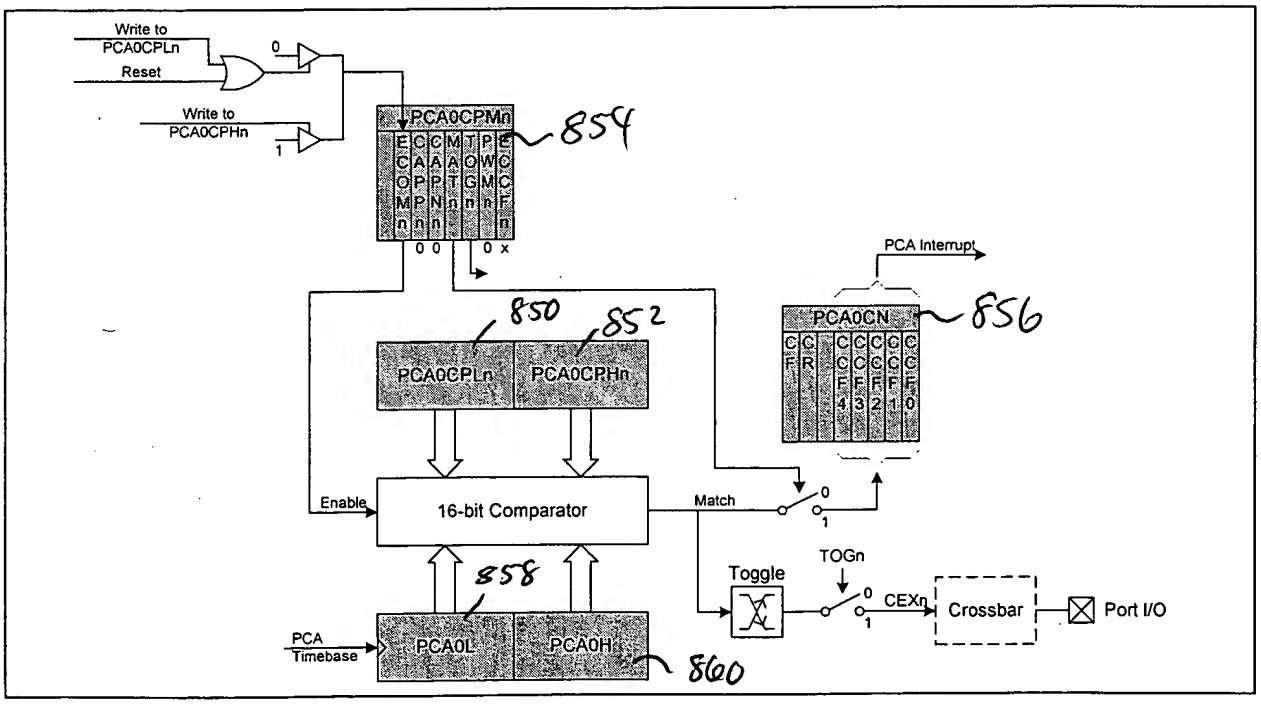


Figure 18.5. PCA High Speed Output Mode Diagram



50

Figure 18.6. PCA PWM Mode Diagram

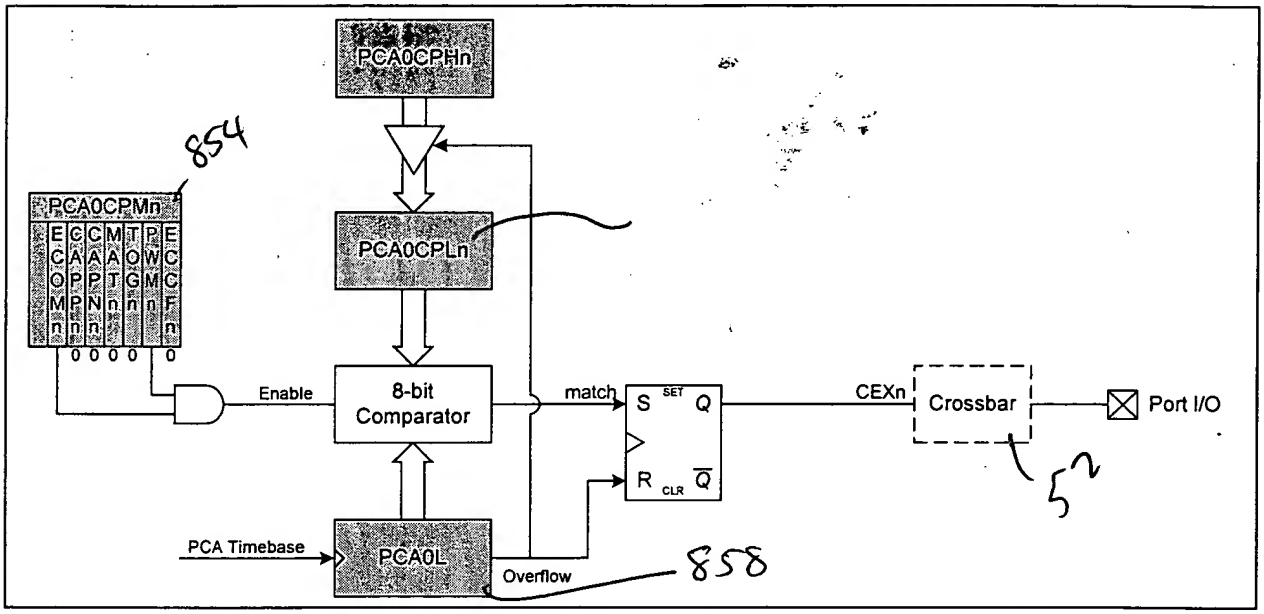


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Figure 18.7. PCA Counter/Timer Block Diagram